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High Efficiency DC-DC Converter with two Input Power Sources using Fuzzy Logic Controller

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***Abstract*—The aim of this study is to develop a high efficiency converter with two input power sources for a distributed power generation mechanism. The proposed converter can boost the varied voltages of different power sources in the sense of hybrid power supply to a stable power output dc voltage for the load demand. An auxiliary circuit in the proposed converter is employed for achieving turn-On zero -voltage switching (ZVS) of all the switches. According to various situations, the operation states of the proposed converter can be divided into two states including a single power supply and a dual power supply. In the dual power supply state, the input circuits connected in series together with the designed pulse width modulation can greatly reduced the conduction losses of the switches. An effective improvement in efficiency can be achieved by using a closed loop "Fuzzy Logic Controller"(FLC) in the proposed topology.**

Index terms -DC-DCconverter,hybridpowersupply,high-efficiencypowerconversion,zero -voltage switching(ZVS).

I. INTRODUCTION

In order to protect the natural environment on the earth, the development of clean energy[1]-[3] without pollution has the major representative role in the last decade. By accompanying the permission of Kyoto Protocol, clean energies, such as fuel cell (FC), photovoltaic (PV), wind energy, etc., have been rapidly promoted. Due to the electric characteristics of clean energies, the generated power is critically affected by the climate or has slow transient responses, and the output voltage is easily influenced by load variations[4]. Thus, a storage element is necessary to ensure proper operation of clean energies.

Batteries or supercapacitors are usually taken as storage mechanisms for smoothing output power, start-up transition, and various load conditions[5].The corresponding installed capacity of clean energies can be further reduced to save the cost of system purchasing and power supply. For these reasons, hybrid power conversion systems (PCS) have become one of interesting research topics for engineers and scientists at present. Based on power electronics technique, the diversely developed power conditioners including dc–dc converters and dc–ac inverters are essential components for clean-energy applications.

Generally, one power source needs a dc–dc converter either for rising the input voltage to a certain band or for regulating the input voltage to a constant dc-bus voltage[6]-[8].However, conventional converter structures have the disadvantages of large size, complex topology, and expensive cost. In order to simplify circuit topology, improve system performance, and reduce manufacturing cost, multi-input converters have received more attentions in recent years [9]-[18].

Liu and Chen [9]proposed a general approach for developing multi-input converters. By analyzing the topologies of converters, the method for synthesizing multi-input converters was inspired by adding an extra pulsating voltage or a current source to a converter with an appropriate connection.

Waiet al. presented multi-input converters with high step-up ratios, and the goal of high-efficiency conversion was obtained. However, these topologies are not economic for the non isolated applications because of the complexity with numbers of electrical components.

Tao et al.[13] and Matsuo et al[14] utilized multi winding-type transformers to accomplish the power conversion target of multi-input sources. Although these topologies were designed based on time-sharing concept, the complexity of driving circuits will be increased by the control techniques.

Marchesoni and Vacca[15] investigated a newly designed converter with the series-connected input circuits to achieve the goal of multiple input power sources. The installation cost of the converter with few components was certainly reduced. The feature of[15] is that the conduction losses of switches can be greatly reduced, especially in the dual power supply state. Unfortunately, the hard-switching problem and the huge reverse-recovery current within the output diode degrade the conversion efficiency as a traditional boost converter[6] .

Kwasinski [16]discussed the evolution of multiple input converters from their respective single-input versions. Based on several assumptions, restrictions, and conditions, these analyses indicate some feasible and unfeasible frameworks for multiple input development. Li et al.[17] investigated a set of basic rules for generating multiple-input

A.HIGH EFFICIENCY DUAL INPUT CONVERTER

In this study, a high-efficiency ZVS dual-input converter is investigated, and this converter directly utilizes the current source type applying to both input power sources. Based on the series-connected input circuits and the designed pulse width modulation (PWM) driving signals, the conduction loss of the switches can be greatly reduced in the dual power-supply state.

Performed zero-current-transition dc–dc converters without additional current stress and conduction loss on the main switch during the resonance period of the auxiliary cell. The auxiliary cell provides zero-current-switching turn-OFF for all active switches and minimizes the reverse recovery problem of the main diode. The modified type of this representative auxiliary cell in is introduced into the proposed dual-input converter to reduce the reverse-recovery currents of the diodes.

An auxiliary circuit with a small inductor operated in the discontinuous conduction mode (DCM) is utilized for achieving turn-ON ZVS of all the switches, and the huge reverse-recovery current of the output diode in the traditional boost converter can be removed via the utilization of an auxiliary inductor series connected with a diode.

Consequently, the proposed dual-input converter can efficiently convert two power sources with different voltages to a stable dc-bus voltage. According to the power dispatch, this converter could be operated at two states including a single power-supply state and a dual power-supply state.

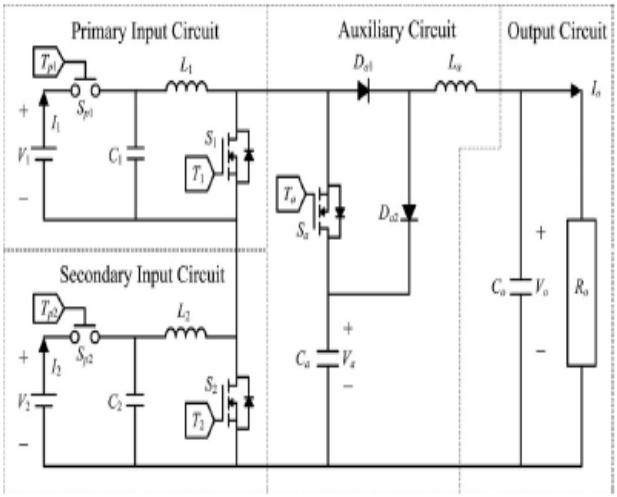

Figure 1. Equivalent circuit of high efficiency dual input converter

II. MODES OF OPERATION

Fig. 1 shows the circuit topology of the proposed ZVS dual input converter. It contains four parts including a primary input circuit, a secondary input circuit, an auxiliary circuit, and an output circuit.

The major symbol representations are summarized as follows. V_1 and I_1 denote the primary input voltage and current, respectively. V_2 and I_2 exhibit the secondary input voltage and current, respectively. SP_1 , SP_2 , TP_1 , and TP_2 express the power ON/OFF switches and their driving signals produced by the power management.

C_i, L_i, S_i, and T_i(i = 1, 2) represent individual capacitors, inductors, switches, and driving signals in the primary and secondary input circuit, respectively. C_a, L_a, Da_1 , and Da_2 are the auxiliary capacitor, inductor, and diodes of the auxiliary circuit. Sa and Ta are the auxiliary switch and its driving signal, which is generated by the PWM. Co , Vo , Io , and Ro describe the output capacitor, voltage, current, and equivalent load, respectively.

The directional definition of significant voltages and currents are labeled in this figure. The simplification is compliant with the following assumptions:

1) All power switches and diodes have ideal characteristics without considering voltage drops when these devices are conducted;

2) The capacitors Caand Co are large enough so that the voltage ripples due to switching are negligible and could taken as constant voltage sources Vaand Vo; and

3) The power ON/OFF switches SP_1 and SP_2 are omitted. According to different power conditions, the operational states of the proposed converter can be divided into two states including a single power-supply state with only one input power source and a dual power-supply state with two input power sources.

The powers produced by the voltage sources V_1 and V_2 are referred as P_1 and P_2 , respectively, while the power consumed by the load is referred as Po . If the condition of $P_1 > P_0 (P_2 > P_0)$ holds, the switch SP_1 (SP_2) turns ON to supply the power with a single input power source V_1 (V_2). On the contrary, the switches SP 1 and SP 2 turn ON to supply the power with two input power sources if the conditions of $P_1 > P_0$and $P_2 > P_0$fail. The detailed operational stages are described as follows.

The auxiliary inductor is also designed to operate in the DCM. In order to explain the operational principle in the dual power supply state easily, the following

theoretical analysis is based on the assumption of $i_{L1} > i_{L2} > |i_{L1} - i_{L2}|$, where $|i_{L1}|$ is the absolute operator. The characteristic waveforms and topological modes of the dual power-supply state are depicted Note that the time intervals in modes 2, 4, 9, and 11 are extremely short so that each interval could be regarded as the same time.

The operation modes in this state are discussed as follows:

***Mode 1 [t0 –t1]*:**At t0, the auxiliary inductor current iLareturned to zero. The switches S1 and S2 are continuously conducted. The auxiliary switch Sa is still turned OFF. Theinductors L1 and L2 are linearly charged by the input voltagesV1 and V2 , respectively.

***Mode 2 [t1 –t2]*:**At t1 , the switch S2 is turned OFF, the switch voltage vS2 is rising to the auxiliary capacitor voltage Va, and the auxiliary switch voltage vSais decreasing to zero. The body diode of the auxiliary switch Sa is iL2 to charge the

auxiliary capacitor. Therefore, the switch current iSais negative. Besides, the auxiliary inductor current iLalinearly increases, and the slope is dependent on the auxiliary inductor voltage vLa, which is equal to Va − Vo . Continuously, the primary auxiliary diode Da1 is conducted.

***Mode 3 [t2 –t3]*:**At t2 , the auxiliary switch Sa is turned ON with ZVS. After the auxiliary inductor current iLaincreases tobe larger than the secondary inductor current iL2 , the auxiliary switch current iSabecomes positive. The discharging current from the auxiliary capacitor together with the secondary inductor current iL2 releases the stored energy to the output voltage Vo . During modes 2 to 3 (t = t1 − t3), the time interval can be written as (dd+ da2)TS . The auxiliary inductor current iLaand the secondary inductor current iL2 can be expressed as

$$iLa(t) = (Va - Vo)(t - t1)La \quad (1)$$

***Mode 4 [t3 –t4]*:**At t3 , the strain. Besides, the auxiliary inductor voltage vLais equal to −Vo , and the current iLalinearly decreases. The energy stored in the auxiliary inductor La starts to discharge into the output voltage Vo as freewheeling.

***Mode 5 [t4 –t5]*:**At t5 , the switch S2 is turned ON with ZVS upon the condition that the auxiliary inductor current iLais still larger than the secondary inductor current iL2 . The auxiliary inductor current iLacontinuously decreases with the slope−Vo/La . After the current iLais smaller than the secondary inductor current iL2 , the switch current iS2 is positive. By the same way, the switch current iS1 becomes positive as well asiS2 . During modes 4 to 5 (t = t3 − t5), the time interval can be written as (dd+ ddcm2)TS . The auxiliary inductor current iLaand the secondary inductor current iL_2 can be expressed as

$$iLa(t) = [(Va - Vo)(dd + da2)TS - Vo(t - t3)]La \quad (2)$$

$$iL2(t) = (IL2 - 0.5\Delta iL2) + V2(t - t3)L2 \quad (3)$$

***Mode 6 [t5 –t6]*:**At t5 , the auxiliary inductor current iLais equal to zero. Substituting iLa(t5) = 0 into (17), the relation between the voltages Vaand Vo can be derived as In this mode, the parasitic capacitor of the primary diode Da1 is charged by the output voltage Vo with a small reverse-recovery current.

***Mode 7 [t6 –t7]*:**At t6 , the diode voltage vDa1 is rising to the output voltage Vo , the secondary auxiliary diode Da2 is conducted for receiving the auxiliary inductor current iLato charge the auxiliary capacitor.

***Mode 8 [t7 –t8]*:**At t7 , the auxiliary inductor current iLareturns to zero. The switches S1 and S2 are continuously conducted. Mode 8 is similar to mode 1.

***Mode 9 [t8 –t9]*:**At t8 , the switch S1 is turned OFF, the switch voltage vS1 is rising to the auxiliary capacitor voltage Va, and the auxiliary switch voltage vSais decreasing to zero. The body diode of the auxiliary switch Sa is conducted for carrying the primary inductor current iL1 to charge the auxiliary capacitor. The auxiliary inductor current iLalinearly increases with the slope (Va − Vo)/La . Continuously, the primary auxiliary diode Da1 is conducted.

***Mode 10 [t9 –t10]*:**At t9 , the auxiliary switch Sa is turned ON with ZVS. After the auxiliary inductor current iLaincreases to be larger than the primary inductor current iL1 , the auxiliary switch current iSabecomes positive. The discharging current from the auxiliary capacitor together with the primary inductor current iL1 releases.

***Mode 11 [t10–t11]*:**At t10, the auxiliary switch Sa is turned OFF. Because the auxiliary inductor current iLais greater than the primary inductor current iL1 , the parasitic capacitor of the stored energy to the output voltage Vo . auxiliary switch Sa is charged by the auxiliary inductor current iLa. At the same time, the energy stored in the parasitic capacitor of the switch S1 will release to the output voltage Vo via the inductor current iLa.

***Mode 12 [t11–t12]*:**At t11, the switch S1 is turned ON with ZVS. The auxiliary inductor current iLacontinuously decreases with the slope −Vo/La . After the current iLais smaller than the primary inductor current iL1 , the switch current iS1 is positive. By the same way, the switch current iS2 becomes positive as well as iS1 . During modes 11 to 12 (t = t10 ∼ t12), the time interval can be written as (dd+ ddcm1)TS . The auxiliary inductor current iLaand the primary inductor current iL1 can be expressed as

$$iLa(t) = [(Va - Vo)(dd + da1)TS - Vo(t - t10)]La \quad (4)$$

$$iL1(t) = (IL1 - 0.5\Delta iL1) + V1(t - t10)L1 \quad (5)$$

Auxiliary switch Sa is turned OFF. Because the auxiliary inductor current iLais greater than the secondary inductor current iL2 , the parasitic capacitor of the auxiliary switch Sa is charged by the auxiliary inductor current iLa, and the auxiliary switch voltage VSarises. At the same time, the energy stored in the parasitic capacitor of the switch S2 will release to the output voltage Vo via the inductor current iLa, and the switch voltage vS2 decreases. The switch current iSafalls down to zero and the switch voltage VSarises to the auxiliary capacitor voltage Va.

***Mode 13 [t12–t13]*:**At t12, the auxiliary inductor current iLais equal to zero. Substituting iLa(t12) =0 , the relation between the voltages Vaand Vo can be derived as

$$(Va- Vo)(dd+ da1) = Vo (dd+ ddcm1) \quad (6)$$

Mode 13 is similar to mode 6 as well as the reverse-recovery time of the primary auxiliary diode Da1 .

Mode 14 [t13–t14]: At t13, the diode voltage vDa1 is rising to the output voltage Vo , and the secondary auxiliary diode Da2is conducted for receiving the auxiliary inductor current iLato charge the auxiliary capacitor.

III. . CLOSED LOOP CONTROL- FLC

In Closed loop, Fuzzy logic starts with the concept of a fuzzy set. A fuzzy setis a set without a crisp, clearly defined boundary. It can contain elements with only a partial degree of membership.

A membership functionis a curve that defines how each point in the input space is mapped to a membership value (or degree of membership) between 0 and 1. The input space is sometimes referred to as the universe of discourse. A fuzzy set admits the possibility of partial membership in it. The degree an object belongs to a fuzzy set is denoted by a membership value between 0 and 1.

A membership function associated with a given fuzzy set maps an input value to its appropriate membership. Fuzzy systems theory enables us to utilize qualitative, linguistic information about a system to construct a mathematical model for it. For many real-life systems, which are highly complex and inherently nonlinear, conventional approaches to modeling are not easy to apply, whereas the fuzzy approach might be a very helpful alternative.

Fuzzy models can be seen as rule-based systems suitable for formalizing the knowledge of experts. Fuzzy control is easy to learn and easy to apply, since it is close to human intuition. Functions are provided for many common methods, including fuzzy clustering and adaptive neuro fuzzy learning.

FLC have some advantages compared to other classical controller such as simplicity of control, low cost and the possibility to design without knowing the exact mathematical model of the process Fuzzy logic is a more intuitive approach without the far-reaching complexity. Structure of a fuzzy logic controller consists of: input, fuzzification.

Rule base, defuzzification, output. There are specific components characteristic of a fuzzy controller to support a design procedure. It shows the controller between the input and output. The inputs are most often hard or crisp measurement from some measuring equipment is converted into fuzzy values for each input fuzzy set with the fuzzification block.

The first block inside the controller is fuzzification which converts each piece of input data to degrees of membership by a lookup in one or several membership functions. The fuzzification block matches the input data with the conditions of the rules to determine.

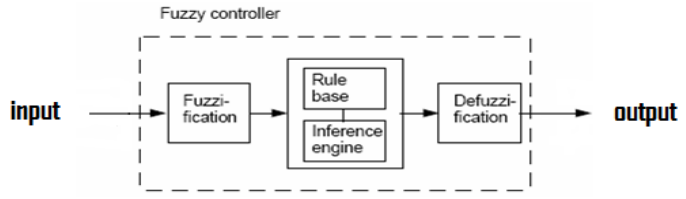

Figure 2. Structure of Fuzzy logic control

The computer is able to execute the rules and compute a control signal depending on the measured inputs error (e) and change in error.(dE). In a rule based controller the control strategy is stored in a more or less natural language. A rule base controller is easy to understand and easy to maintain for a non- specialist end user and an equivalent controller could be implemented using conventional techniques

Defuzzification is when all the actions that have been activated are combined and converted into a single non-fuzzy output signal which is the control signal of the system. The output levels are depending on the rules that the systems have and the positions depending on the non-linearity's existing to the systems.

To achieve the result, develop the control curve of the system representing the I/O relation of the systems and based on the information; define the output degree of the membership function with the aim to minimize the effect of the non-linearity and the output is output gain that can be tuned and also become as an integrator .The output crisp value can be calculated by the centre of gravity or the weighted average.

In our proposed system, by dynamically calculating the nodes trust vector values, the source node can be able to select the more trusted routes rather than selecting the shorter routes. Our system marks and isolates the malicious nodes from participating in the network. So the potential damage caused by the malicious is reduced.

Let $\{Tv_1, Tv2\ldots\}$ be the initial trust vectors of the nodes $\{n_1, n2\ldots\}$ along the route R1 from a source S to the destination D.

Since the node does not have any information about the reliability of its neighbors in the beginning, nodes can neither be fully trusted nor be fully distrusted. When a source S want to establish a route to the destination D, it send route request (RREQ) packets .

When the destination D receives the accumulated RREQ message, it measures the number of packets received Prec. Then it constructs a route on Prec with the key shared by the sender and the destination. The RREP contains the source and destination ids, the route of Prec, the accumulated route from the RREQ,which are digitally signed by the destination. The RREP is sent towards the source on the reverse route R1.

The intermediate node then verifies the digital signature of the destination node stored in the RREP packet, is valid. If the verification fails, then the RREP packet is dropped. Otherwise, it is signed by the intermediate node and forwarded to the next node in the reverse route.

When the source S receives the RREP packet, if first verifies that the first id of the route stored by the RREP is its neighbor. If it is true, then it verifies all the digital signatures of the intermediate nodes, in the RREP packet. The digital signature includes recommendation about the neighbor node and probability that data packet received successfully. If all these verifications are successful, then the trust counter values of the nodes are incremented as

$$Tv_i = Tv_i + \alpha_1 \quad (1)$$

If the verification is failed, then

$$Tv_i = Tv_i - \alpha_1 \quad (2)$$

Where α_1 is the step value, which can be assigned a small fractional value during simulations. After this verification stage, the source S check the digital signature values DS of the nodesn_i.

Digital Signature includes recommendation about the neighbor node and probability that data packet received successfully.

Evaluating the recommendation is given by R_B^A which is node A's evaluation to node B by collecting recommendations

$$R_B^A = \frac{\sum_{v\in\gamma} V|A\rightarrow C| * V|C\rightarrow B|}{V|A\rightarrow C|}$$

γ is a group of recommenders.

$V|A\rightarrow C|$ is trust vector of node A to C.

$V|C\rightarrow B|$ is trust vector of node C to B.

Probability that data packets received can be defined by,

$P_B^A = (1-p_{A,B}) * (1-p_{B,A})$

$p_{A,B}$ is packet loss probability from node A to node B, while , $p_{B,A}$ is packet loss probability from node B to node A.

For any node n_k, if $DS_k<DS_{min}$, where DS_{min} is the minimum threshold value, its trust vector value is further decremented as

$$Tv_i = Tv_i - \alpha_2 \quad (5)$$

For all the other nodes with $DS_k>DS_{min}$, the trust counter values are further incremented as

$$Tv_i = Tv_i + \alpha_2 \quad (6)$$

Where α_2 is another step value with $\alpha_2<\alpha_1$.

For a node n_k, if $Tv_k<Tv_{thr}$, where Tv_{thr} is the trust threshold vector value, then that node is considered and marked as malicious. If the source does not get the RREP packet or RERR packet for a time period of t seconds, it will be considered as a node failure or link failure. Then the route discovery process is initiated by the source again.The same procedure is repeated for the other routes R2, R3 etc and either a route without a malicious node or with least number of malicious node, is selected as the reliable route.

IV. SIMULATION DIAGRAM& RESULTS

Ta are the auxiliary switch and its driving signal, which is generated by the PWM. Co , Vo , Io , and Ro describe the output capacitor, voltage, current, and equivalent load, respectively. It provides tools to create and edit fuzzy inference systems. Allows integrating fuzzy system into simulation with Simulink. It is possible to create stand alone C programs that call fuzzy system built with MATLAB. The tool box provides three categories of tools. They are as follows

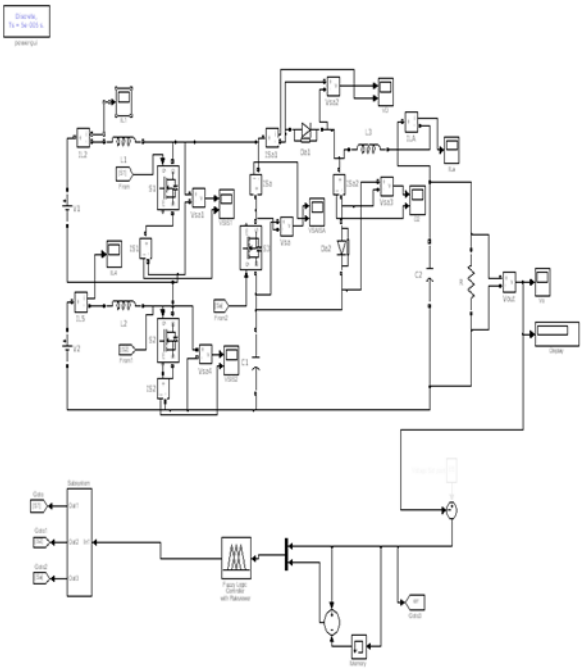

Figure 3 Simulation Diagram with using FLC

i)Command line functions

ii)Graphical or Interactive tools

iii)simulink blocks

The main difficulty in the mathematical analysis of fuzzy models is that they are inherently nonlinear and, therefore, classical control theory with its emphasis on linear systems is difficult to apply or cannot be applied at all. Multiple-input and single-output rule-based system considered in it. A membership function associated with a given fuzzy set maps an input value to its appropriate membership. Fuzzy systems theory enables us to utilize qualitative, linguistic information about a system to construct a mathematical model for it.

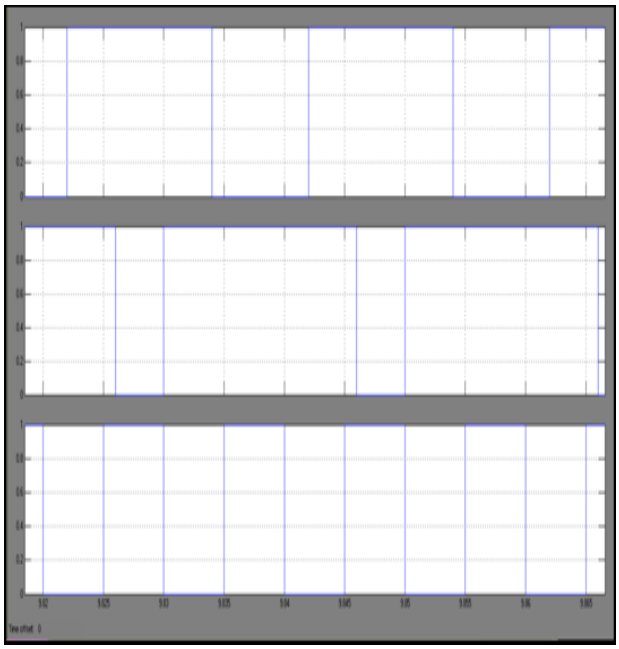

Figure 4. Triggering Pulse For S_1,S_2,S_3

For many real-life systems, which are highly complex and inherently nonlinear, conventional approaches to modeling are not easy to apply, whereas the fuzzy approach might be a very helpful alternative. The collection of rules is called the rule base. The rules are in "IF THEN" format and formally the IF side conditions.

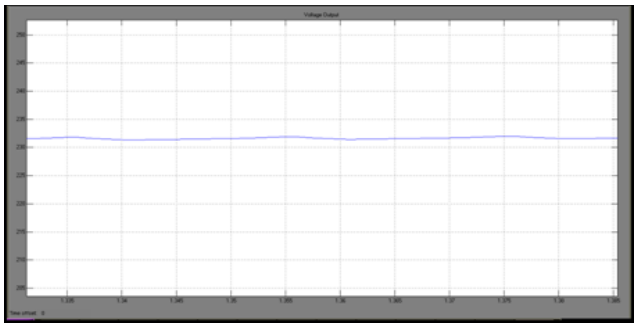

Figure 5 Output Voltage Without Controller

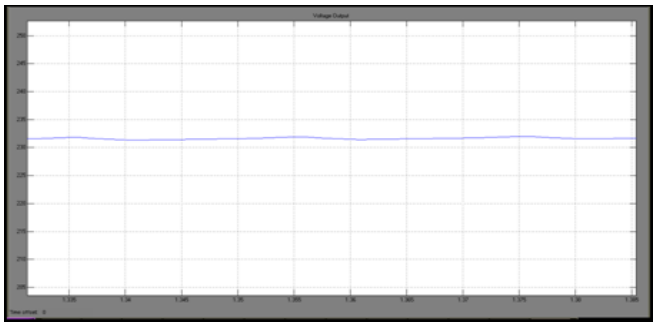

Figure 6 Voltage Waveform For FLC

From the figure 5 and figure 6,the output voltage waveform, both the single and dual power supply state under FLC efficiency is approximately 95%,that means it is a "stable dc output".

V.MODEL CALCULATION

FOR DUAL SUPPLY WITHOUT FEEDBACK

$Efficiency_2$ = Output power/ Input Power

=(1.9 * 10^3)/(2.2 *10^3)=86.3%

$Efficiency_1$ = Output power/ Input Power

= (2*(10^3))/(2.2 * 10^3) = 90.9%

$Efficiency_2$ / $Efficiency_1$ = 86.3/90.9 = 94.93%

FOR DUAL SUPPLY WITH FLC

$Efficiency_2$ = Output power/ Input Power

=(1.94* 10^3)/(2.2 *10^3)=88.18%

$Efficiency_1$ = Output power/ Input Power

= (2*(10^3))/(2.2 * 10^3) = 90.9%

$Efficiency_2$ / $Efficiency_1$ = 88.18/90.9 = 97%.

VI. CONCLUSION

This study has successfully developed a ZVS dual-input converter with hybrid power. In the dual power-supply state, the conduction loss can be effectively reduced by topological design of series connection of two input circuits. Besides, the reverse-recovery currents of the diodes are slight as well as the switching losses of the switches are effectively reduced. The maximum efficiency of the proposed converter operated in both operational states is higher than 95%. If the proposed ZVS dual-input converter in this study is used for non-isolated PV applications, the ground leakage current issue due to the high-frequency voltage swing occurs which could be solved by the adoption of an EMI filter for a dc power supply application or the integration with advanced inverter topologies for an ac-module application in the future research.

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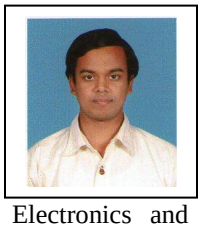
Authors Profile



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