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FPGA based rrc filter using distributed arithmetic Algorithm

Monika Singh
NITTTR Chandigarh

Dr. Rajesh Mehra
NITTTR Chandigarh

Abstract

RRC filters are used to avoid the intersymbol interference in wireless communication. This paper present design and implementation of Root Raised Cosine (RRC) filter using distributed arithmetic algorithm. Distributed Arithmetic is multiplier less approach that uses look up tables (LUT) of target FPGA. It eliminates the use of multipliers in hardware implementation. The proposed reconfigurable root raised cosine (RRC) filter has been designed and simulated using MATLAB and Xilinx ISE. The synthesis has been performed on Spartan3E XC3500e and Virtex-2-pro XC2VP30 target FPGA. The proposed structure can operate at an estimated frequency of 189.88 MHz as compared to existing frequency 146.5 MHz in case of RRC filter using DA algorithm to provide cost effective solution.

Key Words: *Raised Cosine, ISI, FPGA, Distributed Arithmetic Algorithm*

I. Introduction

Today's consumer electronics such as cellular phones and other multi-media and wireless devices often require digital signal processing (DSP) algorithms for several crucial operations [1]. Application of digital signal processing uses the variable sampling rates which can improve the flexibility of Software Defined Radio (SDR). It reduces the anti-aliasing analog filters and enables processing with different sampling rate. The demand for such a complex DSP applications, high performance, low cost SOC implementations of DSP algorithm are getting increased attention among researchers and design engineers [2]. Digital signal processor (DSP) systems are increasingly being implemented on field programmable gate array (FPGA) hardware platforms [3]. FPGA provide a reconfigurable solution for implementing DSP applications as well as higher DSP throughput and raw data processing power than DSP processors. There is a unceasing requirement for efficient use of FPGA resources where occupying less hardware for a given system that can produce significant cost-related benefits.

(i) reduced power consumption;
(ii) area for additional application functionality;
(iii) potential to use a smaller, cheaper FPGA.

On one hand, high development costs and time-to-market factors associated with ASICs can be prohibitive for certain applications while, on the other hand, programmable DSP processors can be unable to meet desired performance due to their sequential-execution architecture. In this case, embedded FPGA offers a very attractive solution that balance high flexibility, time to market , cost and performance [4]. In many cases, FPGAs work in conjunction with a conventional DSP as integrating pre and post-processing functions, along with high performance signal processing. Finite impulse response (FIR) digital filters are functions and are generally used in FPGA implementations. If very high sampling rates are required, full-parallel hardware must be used where every clock edge feeds a new input sample and produces a new output sample. Such filters can be implemented on FPGAs using combinations of the general purpose logic fabric, on-board RAM and embedded arithmetic hardware. FPGA is advancing rapidly as a highly important element of the future of computing. Already developments have shown that it can massively reduce the price of specialized system development and it can compete on a variety of attributes with top range commercially available microprocessors. A traditional DSP chip would perform the MAC FIR Filter function in serial manner where as an FPGA allows designers to implement this function in parallel style using dedicated multipliers and registers that are now available in recent FPGAs. The main advantage of FPGAs is their architectures which are well suited for highly parallel implementation of DSP functions to enhance the system performance. User programmability also allows designers to trade-off device area Vs. performance by selecting the appropriate level of parallelism to implement their functions. The other advantage of FPGA is its ability to integrate system logic.

The work in this paper presents the design and implementation of Raised cosine filter target as virtex2p FPGA using Distributed Arithmetic Procedure. The results of the implementation experiment are analysed in terms of area and speed. The brief description of the RRC filter is presented in Section 2. Discussion of DA algorithm in section 3.The proposed design and simulation for RRC filter presented in section 4. Results and discussion present in section 5. Then, the concluding remarks are given.

2. RRC Filter

pulse shaping filters are used to keep the signal are allotted bandwidth, maximize the data transmission rate and minimize the transmission errors. It is the heart of many modern data transmission rate like HDTV, mobile phones [5]. To avoid the intersymbol interference root raised cosine filters are used and for data rate transmission constrain amount of bandwidth are required. Pulse shaping filter are the example of root raised cosine filter and RRC is a favorable filter to do pulse shaping as it transition band is shaped like a cosine curve and the response meets the nyquist Criteria [6]. The nyquist criterion states that in order to achieve an ISI-free transmission, the impulse response of the shaping filter must have zero crossings at multiples of the symbol period. A time-domain sinc pulse meets these requirements, since its frequency response is a brick wall but this filter is not realizable [7]. We can also estimate it by sampling the impulse response of the ideal continuous filter. The sampling rate must be at least twice the symbol rate of the message to transmit. So the filter must be interpolate the data by at least a factor of two and often more to simplify the analog circuitry. It is a simplest system configuration, a pulse shaping interpolator at the transmitter is associated with a simple down sampler at the receiver. The FIR structure with linear phase technique is efficient as it takes advantage of symmetrical coefficients and uses half the required multiplications and additions [8]. So this paper focuses on efficient design of DUC on an FPGA target device.

3. DA ALGORITHM

Distributed Arithmetic Algorithm (DA) plays an vital role in embedding DSP functions in the Xilinx family of FPGA devices. Distributed Arithmetic, beside with Modulo Arithmetic, are the efficient technique that provide the computation algorithms which perform multiplication with look-up table based on the schemes. This technique, first proposed by Crosiers is a multiplierless architecture that is based on an efficient partition of the function in partial terms using 2's complement binary representation of data. It is used for Multiplication operations to replace MAC operations. It uses look-up tables and accumulators instead of multipliers for computing inner products. So it provides multiplier less MAC operations [9]. Since DA is a multiplierless technique; so the addition operation of the system is increase in speed. Consequently minimizing the need of addition operation while processing the input signal is of great importance. This aim is apparent with a modification and optimization algorithm proposed to minimize the number of non-zero coefficient used to represent the FIR frequency response. The modification algorithm is applied for different raised cosine FIR filters [10]. Distributed arithmetic techniques are widely used to implement Sum-of-Products computations such as the calculations found in multimedia applications like FIR filtering and discrete cosine transform. In DA, multiplications are rearranged and mixed such that the arithmetic becomes distributed. When DA is implemented in FPGAs, one can take advantage of memory in FPGAs to implement the MAC operation [11]. The main operations are required for DA based computation is its inner product which is a sequence of look up table (LUT) followed by shift accumulator operation of LUT output. For FPGA realization, DA based computation is well suited, because the LUT as well as the shift add-operations, which can be efficiently mapped into the look up table (LUT) based FPGA logic structure [6, 9]. The arithmetic sum of product that defines the response of linear time-invariant (filters) can be expressed as follow.

$$y = \sum_{k=1}^{k} A_k X_k \quad (1)$$

Let X_k be an N-bit scaled two's complement number.

$$X_k = -b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \quad (2)$$

Substituting equation (2) in (1)

$$y = \sum_{k=-1}^{k} A_k \left[-b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n}\right]$$

$$y = -\sum_{k=1}^{k} (b_{k0} . A_k) + \sum_{k=1}^{k} \sum_{n=1}^{N-1} (A_k\ b_{kn}) 2^{-n} \quad (3)$$

$$y = -\sum_{k=1}^{k} A_k b_{k0} + \sum_{n=1}^{N-1} [\sum_{k=1}^{N-1} A_k\ b_{kn}] 2^{-n} \quad (4)$$

4. Proposed Design Simulation

The raised cosine filter is obtained by using the analytical impulse response and it results in higher filter order. The proposed Raised Cosine filter has been designed using Matlab and Xilinx in which taking filter order 24 and roll off factor 0.5. The design is an efficient realization of RRC filter using two logic families Spartan 3E and Virtex 2P target FPGA. In this simulation Distributed Arithmetic Algorithm is used, DA techniques gives the multiplier less results. As per already simulated result response of Gaussian window is better than Kaiser Window [6]. Figure 1 Show the magnitude response of RRC filter and figure 2 Show the impulse response of RRC filter by using Gaussian window. Distributed Arithmetic (DA) approach based on bit- serial access, where arithmetic operation is not

lumped in familiar fashion such as a multiplier but is distributed, have been widely adopted for implementation [12].

specially designed to meet the needs of high volume, cost sensitive consumer electronics application.

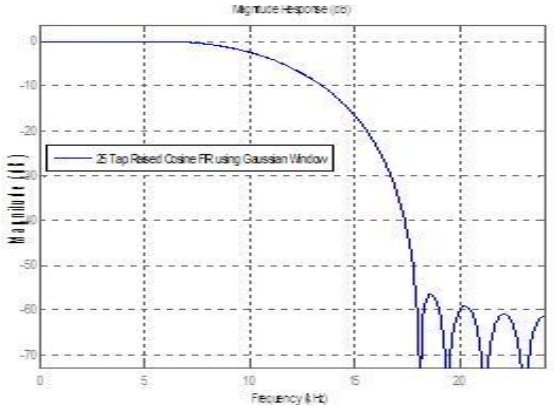

Fig. 1 Magnitude response of RRC Filter

Spartan 3E family builds on the success of the earlier Spartan 3E family by increasing the amount of logic per input-output, which reducing the cost per logic cell. Virtex 2P Development System provides an advanced hardware platform that consists of a high performance Virtex 2P Platform FPGA surrounded by a comprehensive collection of peripheral components that can be used to create a complex system and to demonstrate the capability of the Virtex 2P Platform FPGA.

Figure 3 Shows the simulation of RRC filter using Virtex 2P

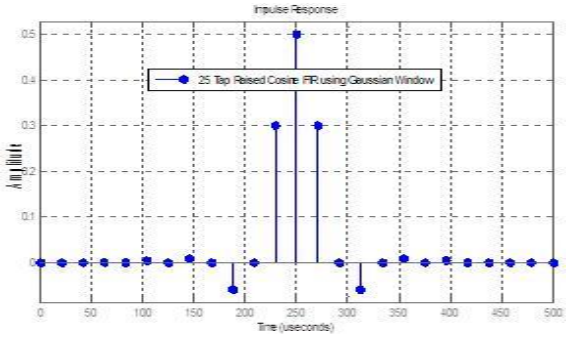

Fig. 2 Impulse response of RRC filter

5. Synthesis Results

After completion the MATLAB simulation the proposed RRC filter has been implemented on Spartan3 and Virtex2p based Xc35500e and Xc2vp30 target FPGA device using distributed arithmetic algorithm. Spartan 3E family of FPGA is

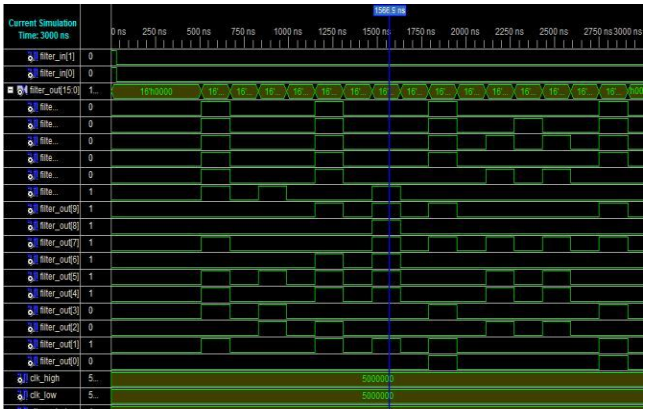

Fig. 3 ISE Simulated based Response

Table 1 Resource Utilization Virtex 2P.

Parameter	Used	Available	Utilization
Number of slices	195	13696	1%
Number of slice flip flops	187	27392	0%
Number of 4 input LUTs	335	27392	1%
Number of bonded IOBs	35	556	6%
Number of GCLKs	1	16	6%

Table 2 Resource Utilization Spartan 3E.

Parameter	Used	Available	Utilization
Number of slices	192	4656	4%
Number of slice flip flops	184	9312	1%
Number of 4 input LUTs	343	9312	3%
Number of bonded IOBs	35	232	15%
Number GCLKs	1	24	4%

The complete simulation of RRC filter by using different

logic families and the results can be shown in form of table. The benefits associated with FPGA such as flexibility, shorter time to market and reconfigurabililty make them a very attractive choice for implementing the designs [13]. Table 1 shows the resource utilization using Virtex 2P, table 2 shows the resource utilization using Spartan 3E and table 3 shows the comparison with existing design. Design and analysis of raised cosine filter is verified by using the Integrated Software Environment, which is the Xilinx software.

Table 3 Resource Comparison

Logic Utilization	Available	Resource Utilization	
		Spartan 3E	Virtex 2P
Number of slices	450	192	195
Number of slice flip flop	101	184	187
Number of 4 input LUTs	544	343	335
Number of DSP Slices	13	_-	-

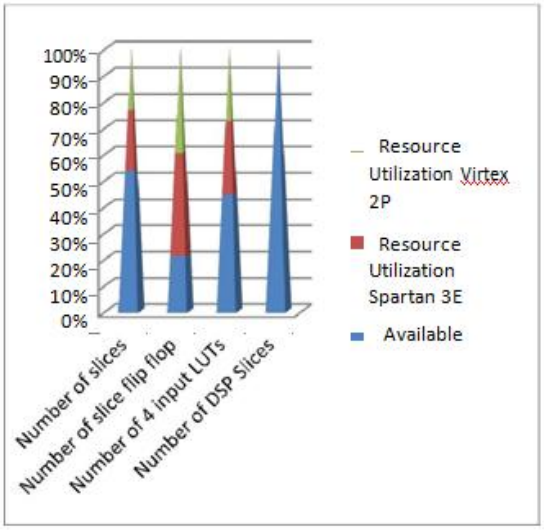

Fig. 4 Comparative Analysis

The proposed Raised cosine filter (RRC) can operate at a maximum frequency of 189.888 MHz with minimum period of 5.266ns based on Virtex 2P target FPGA. The distributed arithmetic algorithm based design of RRC filter has consumed only 195 numbers of slices, 187 number of slice flip flops, 335 numbers of LUTs and no use of any multipliers. Number of DSP slices used in available design but not used in existing design due to utilization of DA, it is multiplier less technique.

Figure.4 shows the resource comparison of two designs Virtex2p and Spartan3E with the existing or available design. In proposed design number of slices, number of flip flops, number of 4 input LUTs less used as compared to two other design.

5. Conclusion

In this paper an efficient approach of Raised Cosine filter has been presented using distributed arithmetic algorithm. DA technique is used to give the better result on its performance. The filter has been designed and implemented by using Spartan 3E and Virtex 2P of target FPGA. The result have shown that the hardware implementation of the proposed filter to improve speed. The proposed filter can be operated at an estimated frequency of 189.88 MHz as compared to existing frequency of 146.5 MHz with minimum period of 4.141 ns by using Virtex 2P. The multiplier less design of RRC filter has consumed only 195 number of slices, 187 number of flip flops, 335 number of 4 input LUTs target FPGA.

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Authors Profile:

Monika Singh: Monika Singh is M.E. scholar from National Institute of Technical Teachers Training and Research, Chandigarh India. She is having five years of teaching experience. She has completed her B.Tech from B abu Banarsi Das Institute of Engineering Technology And Research Center from Uttar Pradesh in 2009. Her interest areas are Digital Signal Processing, VLSI Design, Digital Electronics, and Wireless Communication.

Dr. Rajesh Mehra: Dr. Mehra is currently associated with Electronics and Communication Engineering Department of National Institute of Technical Teachers' Training & Research,Chandigarh, India since 1996. He has received his Doctor of Philosophy in Engineering and Technology from Panjab University, Chandigarh, India in 2015. Dr. Mehra received his Master of Engineering from Panjab Univeristy, Chandigarh, India in 2008 and Bachelor of Technology from NIT, Jalandhar, India in 1994. Dr. Mehra has 20 years of academic and industry experience. He has more than 250 papers in his credit which are published in refereed International Journals and Conferences. Dr. Mehra has 55 ME thesis in his credit. He has also authored one book on PLC & SCADA. His research areas are Advanced Digital Signal Processing, VLSI Design, FPGA System Design, Embedded System Design, and Wireless & Mobile Communication. Dr. Mehra is member of IEEE and ISTE.