Evalution Of Vlsi Design To Obtain Zero Power Dissipation

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ABSTRACT :

Reversible logic circuits have been implemented. This paper deals with the efficient carry skip adder and carry skip BCD adder using reversible circuits. The main advantage of using reversible logic gates in our architecture is that there is no loss of information.

KEY WORDS :

Carry Skip Adder, Carry Skip Binary Coded Decimal Adder, Reversible logic, No Loss Of Information, Zero Power Dissipation.

INTRODUCTION :

The major drawback of complex circuits is the power dissipation. The irreversible circuits suffers from loss of information . Obtaining zero dissipation circuit is only possible by applying the principle of reversibility. So due to this advantage in the upcoming circuit design this reversibility concept will have a major role. The most common numbering system in computer is binary numbering system. But the representation of fractions interms of binary number is quite complex. Inorder to overcome this complexity Binary Coded Decimal (BCD) system was introduced. Adders are the basic function in many calculations. There are several types of adders available in Binary system such as ripple carry adder, carry propagate adder, carry skip adder etc.This increases the delay. The carry look ahead adder proposed parallelism concept for calculating the carry bit. But still there is some time delay in the circuit. The carry skip adder overcomes this drawback by skipping the carry bits over some stages and thus producing garbage outputs.In this paper we will study about the gate counts, garbage outputs and constant inputs proposed in[1].

1.1. BASIC DENOTATION :

1.1.1.Reversible Gate :

Reversible gates are the gates in which number of inputs (i) is equal to the number of outputs(o) in the sense of one to one correspondence between the input and output. These circuits provide unique output pattern. As mentioned earlier the reversible logic gates provide low power consumption.

1.1.2. Garbage Output :

To overcome the power dissipations in quantum computing ,optical computing and low power digital circuits,

The garbage outputs are the one which are not used in the circuits but it has its influence in the performance of the circuit. Due to this reason the the usage of garbage outputs in the circuit should be reduced. But these outputs help in maintaining the reversibility logic in the circuit. In other words its simply the unused outputs of the reversible gate.

1.1.3. Constant Input :

The number of input setted to the circuit to maintain the reversibility of the circuit is known as constant input. The applied input can either be zero(0) or one(1). When the input is set as ‘low’ or ‘0’ as constant then we can obtain an copy of applied input bits. On other hand if the input is set as ‘high’ or ‘1’ as constant then we can obtain the inverted input bit.

1.1.4. Quantum cost :

The number of basic reversible gates (gates of which cost is already known) needed to realize the circuit is known as quantum cost.

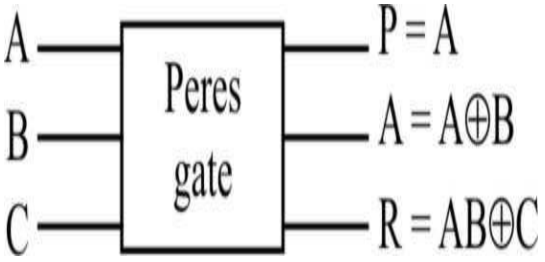
1.1.5. Restrictions on reversible logic concept :

The various parameters like fan-out, loop or feedback is limited strictly in this reversible logic. Anyways by using of additional gates like BVF and FG these can be obtained.

SOME OF THE GATES USED:

1.1.6.Reversible Peres Gate (PG)

The 3×3 (Peres, 1985) is given as:



The input variables are A,B and C and output variables are

P =A,

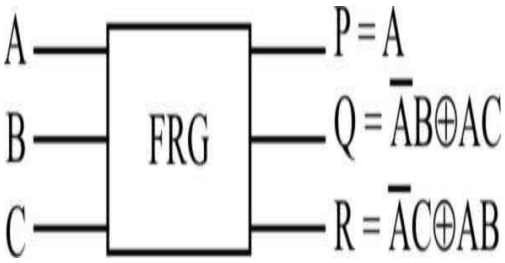
Q = A⊕B,

R = AB⊕C.

Peres Gate (PG) is the mixture proposed in [2] and [3]. This is basically used for performing AND operation.

1.1.7. Reversible Fredkin Gate (FRG)

FRG gate is depicted as

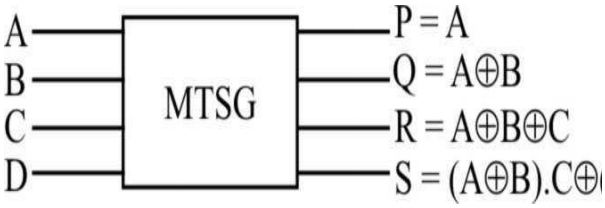


The input variables are A, B and C.
The output variables are
P = A,
Q = B⊕AC,
R = C⊕AB
The FRG circuit is used in [4] for performing carry ripple and carry skip adder circuits. This is used for performing AND and OR operations.

1.1.8. Reversible MTSG Gate

The MTSG gate is proposed in [6].

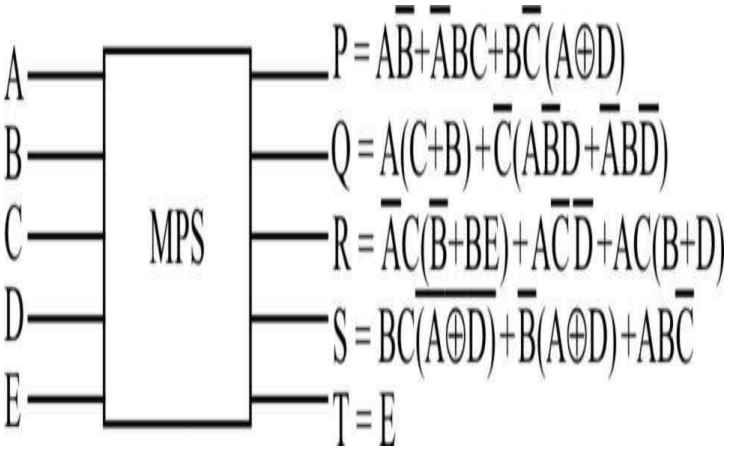
Modified TSG (MTSG) gate is a 4×4 reversible gate. It is described as



The input variables are represented A, B, C& D. The output variables are represented as follows
P=A
Q= (A⊕B)
R= A⊕B⊕C and
S = (A⊕B). C⊕(AB⊕D)
By setting the input value of D as '0' we can obtain basic adder logic

1.1.9. MPS Gate

The 5x5 MPS reversible gate is represented as follow



The five input variable are represented as A, B, C, D & E.
And the output variable are represented as P, Q, R, S & T.
If the output is greater than 9(1001) then the gate corrects it with a correction factor 6(0110) to produce the BCD output.

MATERIALS AND METHODS:

Carry Skip Adder Architecture:

In the proposed carry skip adder in **Fig. 1**, 32 bit parallel addition is done by the modified TSG (MTSG) gate. The three Peres gate is used to generate the propagate signal Z, where Z0 =P0P1P2P3 , Z1= P4P5P6P7, Z2=P8P9P10P11, Z3=P12P13P14P15, Z4=P16P17P18P19, Z5=P20P21P23P24, Z6=P21P22P23P24, Z7=P25P26P27P28, Z8=P29P30P31P32. In which the P0 to P7 is obtained as, Pi = Ai⊕Bi, where i=0,1,2,...30,31.

Toffoli gate can also be used as an alternative for Peres gate for this logic. But in this circuit Peres gate is preferred because of lower quantum cost when compared to Toffoli gate. The combined AND-OR function i.e., Cout = ZCin + Cj, where j=4,8,12,16,20,24,28,32 is produced by using fredkin gate.

Algorithm:
Reversible Carry-skip-adder (A, B, Ci)
Input:
Input Vectors: A = (A_{31},A_{30},A_{29}, . . . , A2,A1,A0) and
B= (B_{31},B_{30},B_{29}, . . . , B2,B1,B0)
Carry input : Cin
Output:
Output Vectors: S = (C_{out8},$C_{out7,}$ . . . ,$C_{out0,}$ S_{31},S_{30},S_{29}, . . . ,S_2,S_1,S_0)
begin
Step1:
Pi output at each stage is given as
for (i = 0 to 31)
{

Pi = Ai ⊕Bi
}
Z = Po AND P1 AND P2 AND P3

Step 2:

Compute Si = Ai⊕Bi⊕Ci for every adder block using the MTSG gate and Ci = (Ai⊕Bi). Cin⊕(AiBi) is generated for each adder block.

Step 3:

Evaluate the final carry output, Cout = ZCin+Cj (Where j = 4,8,12,16,20,24,28,32)

end

Carry Skip BCD Adder Architecture:

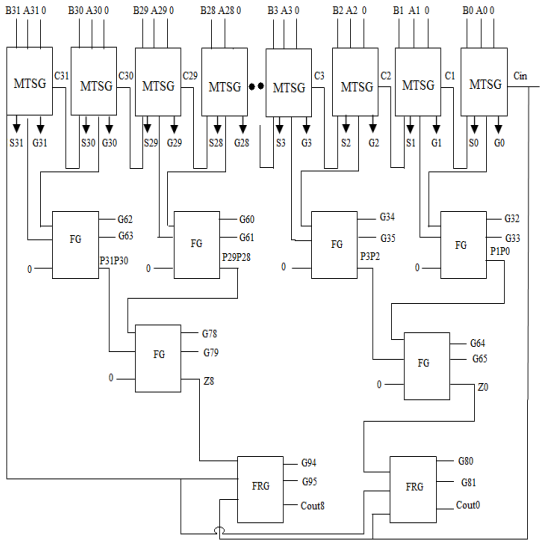


FIG.1. PROPOSED CARRY SKIP ADDER (32 BIT)

****NOTE:** FIG.2 is for 4bit, extend it in the same way as 32 bit carry skip adder (as shown in fig.1) and in addition add MPS gate at the end and the input for those gates is the output 'S' from MTSG gates and Cout from FRG respectively.

POWER ANALYSER:

CARRY SKIP ADDER:

D	E	F	G	H
On-Chip	Power (W)	Used	Available	Utilizati
Logic	0.000	72	7168	
Signals	0.000	106	---	
IOs	0.000	115	141	
Leakage	0.060			
Total	0.060			

CARRY SKIP BCD ADDER:

The fig.2 represents the proposed reversible carry skip BCD adder. This architecture follow the basic architecture as we designed for the carry skip adder. But in this there is an addition block inorder to detect and correct the BCD overflow. In addition to its sum and carry bit MTSG block is used for its parallel addition and produce propagate bits (P0,P1, . . . ,P30,P31). The Sout output is obtained by 'Z' output from FG gate. The Cout value as we obtained in fig.1 is similar to the Sout output in fig.2. The gate used for BCD detection and correction is a MPS gate and it produce the BCD SUM.

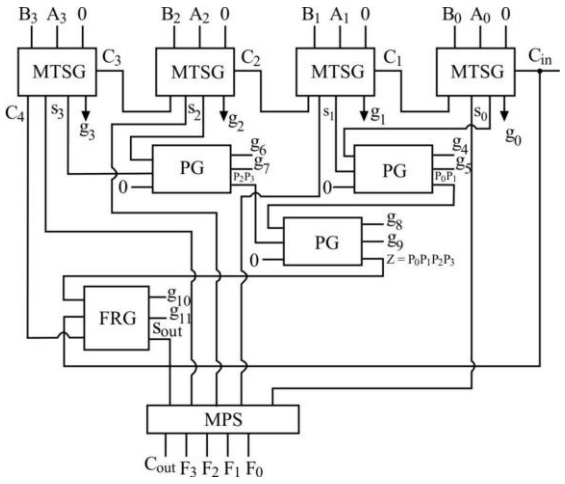


FIG.2. CARRY SKIP BCD ADDER

D	E	F	G	H
On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	92	7168	1
Signals	0.000	123	---	---
IOs	0.000	135	141	96
Leakage	0.060			
Total	0.060			

CONCLUSION :

In the study an optimized carry skip adder and carry skip BCD adder are presented. It is clearly found that both circuits are highly optimized in terms of gate count, constant input and garbage output when compared with the existing designs. These optimized parameters will have a direct effect on the total cost of the circuit. These types of adders will be definitely useful in constructing larger computational structures and in future computers.

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