Efficient Floor Planning to Reduce Thermal Dissipation in 3D-ICs

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***Abstract*— Thermal analysis is essential in 3D-IC technology due to the reduced footprint and higher power densities compared to conventional 2D packaging. We report reduction of the thermal dissipation in 3D-ICs by efficient layer assignment in an algorithm. The algorithm is hybrid of simulated annealing. B*Tree has been used to optimize area and power which increase the speed and reliability and reduce the power consumption. It is also tested on thermal modeling HOTSPOT 5.0 and experimental result based on Alpha benchmark that algorithm can optimize thermal dissipation.**

The experiment use simulated annealing and B*Tree as hybrid algorithm for reduce thermal dissipation in 3D-IC. It simulated on Intel® Pentium® CPU 2020M @ 2.40 GHz PC with 4GB RAM. The result shows 28.23% average temperature decrease and 0.625% of total width and height reduce and total area also reduce is 1.1328%.

Index terms - HOTSPOT 5.0, 3D-ICs, B*Tree, Floor Plan.

I. INTRODUCTION

3D-ICs is becoming a hot issue and future of electronics because of its potential of enhancing performance, while it is also facing challenges such as the increased thermal dissipation on floor planning in VLSI domain. Traditional scaling of semiconductor chips also improves signal propagation speed. However, scaling from current manufacturing and chip-design technologies has become more difficult, in part because of power-density constraints, and in part because interconnects do not become faster while transistors do. 3-D integrated circuits were invented to address the scaling challenge by stacking 2-D dies and connecting them in the 3rd dimension [1-5]. This promises to speed up communication between layered chips, compared to planar layout.

The concerns at rising trends in accurate thermal-conscious mechanisms and the impact of variations due to design uncertainty in early planning stage of a chip fabricated with sub-micron technologies. Designers are looking at developing new methods to tackle these problems at an early design stage so that unnecessary work may be avoided at later stages. Floor planning has been a major focus of attention and research since it can impact many important design decisions at an early stage. Many thermal-aware floor planners exist that estimate the temperature of the chip and help to reduce hotspots by clever floor planning techniques. However, with the onset of high switching activity circuits i.e. circuits which have high usage of specific interconnects and increasing interconnect power dissipation, previous floor planners fail to provide accurate temperature estimates. Thus, our problem definition consists of developing a floor planning algorithm with the objective of minimizing thermal effect [2-6]. We present efficient 3D-ICs optimization of thermal dissipation in new circuit designs.

II. 3D-IC

A three-dimensional integrated circuit (3D-IC) is a chip in which two or more layers of active electronic components are integrated both vertically and horizontally into a single circuit as shown in Fig-1.

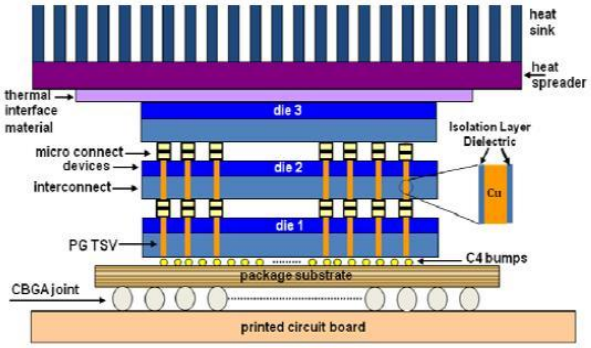

Fig 1: 3D-IC

3D ICs promise many significant benefits like more functionality fits into a small space, cost effective, circuit layers can be built with different processes, or even on different types of wafers, shorter interconnect, low power consumption, vertical dimension adds a higher order of connectivity and offers new design possibilities, and allows large numbers of vertical vias between the layers which allows construction of wide bandwidth buses between functional blocks in different layers.

III. FLOOR PLANNING AND ALGORITHM

General floor plan is similar to mosaic floor plan in that non-slicing structures are allowed. However, the floor plan region can be dissected into more than *n* rooms such that some rooms are empty, i.e. not occupied by any block as in Figure-2.

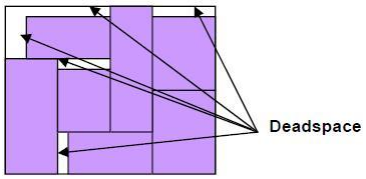

Fig.2: General Floor plan.

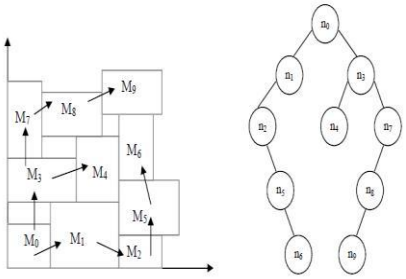

Fig 3(a) & (b) placement and its corresponding B*-Tree

Dead space of a floor plan is the space that is wasted as shown in Fig-2. Minimizing area is the same as minimizing dead space. Dead space percentage is computed as

$$\frac{(1-\sum_{i=1}^{n} A_i)}{A} \times 100\% \quad (1)$$

Where *Ai* is the area of each block *i* and *A* is the total area of the floor plan.

Slicing floor plan is a special case of mosaic floor plan and mosaic floor plan is a special case of general floor plan. As the number of feasible solutions for a given instance of a floor planning problem is very large, floor planning algorithms use cost function as a measure that allows selecting superior floor plans with specific criteria. The possible criteria may be minimizing area, wire length, delays, optimizing routing structure, power density and temperature of the chip or a combination of two or more of the above criteria. The specific criterion ensures greater reliability and performance of the circuits [21, 22]. A commonly used objective function is a weighted sum of area and wire length:

$$Cost = \alpha \times A + \beta \times L \quad (2)$$

Where A is the total area of the packing, L is the total wire length, and α and β are constants.

Chang et al. presented a binary tree based representation for a left and bottom compacted placement called B*-Tree and showed its superior properties for operations [18]. Given a placement P, we can construct a unique B*-Tree in linear time by using a recursive procedure similar to the depth first search (DFS) algorithm. Each node *ni* in a B*-Tree denotes a module. The root of a B*-Tree corresponds to the module on the bottom-left corner. The left child n_j of a node n_i denotes the module m_j that is the lowest adjacent module on the right-hand side of m_i

i.e. $x_j = x_i + w_i$ (3)

The right child n_k of a node n_i denotes the module m_k that is the lowest visible module above m_i and with the same x co-ordinate as m_i i.e.

$$x_k = x_i \quad (4)$$

Figures-3(a) & (b) shows a placement and its corresponding B*-Tree respectively. The root n_0 of the B*-Tree in Figure-3(b) denotes that m_0 is the module on the bottom-left corner of the placement. For node n_3 in the B*tree, n_3 has a left child n_4 which means that module m_4 is the lowest adjacent module in the right-hand side of module m_3 (i.e. $x_4 = x_3 + w_3$). n_7 is the right child of n_3 since module m_7 is the visible module over module m_3 and the two modules have the same x co-ordinate ($x_7 = x_3$).

IV. HOTSPOT AND HOTSPOT TOOL

Hotspot is an accurate and fast thermal model suitable for use in architectural studies. It is based on an equivalent circuit of thermal resistances and capacitances that correspond to micro architecture blocks and essential aspects of the thermal package. The model has been validated using finite element simulation. Hotspot has a simple set of interfaces and hence can be integrated with most power-performance simulators like Wattch. The chief advantage of hotspot is that it is compatible with the kinds of power performance models used in the computer architecture community, requiring no detailed design or synthesis description. Hotspot makes it possible to study thermal evolution over long periods of real, full-length applications [8,9].

We have used Hotspot 5.0 in our experiments. The same Alpha processor (0.13μm technology) floor plan used by Skadron is used in our experiments (shown in Figure-4). We use 24 benchmarks from the SPEC 2000 suite in our experiments [10].

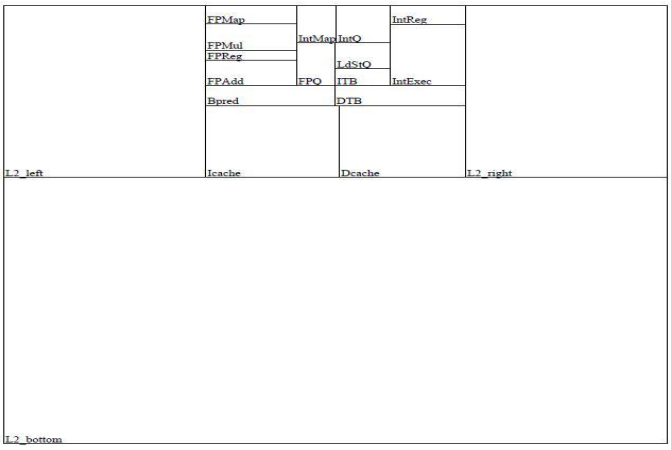

Fig 4 The alpha floorplan

The temperature and power density of each processor block for the *gcc* benchmark are shown in Figure-5. We do not show the temperature of the L2 cache in the figure because the L2 cache has a considerably lower temperature than the other blocks in the processor core.

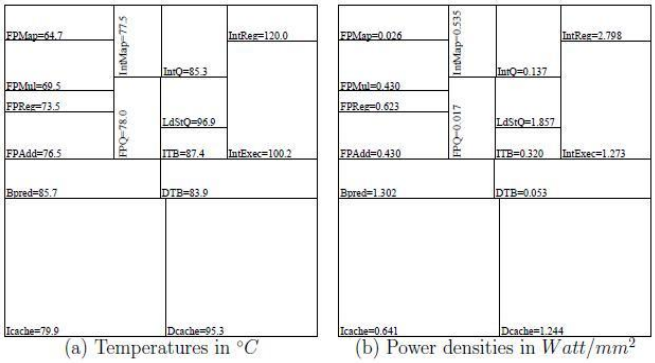

Fig 5: Temperatures and power densities for *gcc* benchmark.

From Figure 5, we can see that the block with the maximum temperature in the chip is the integer register ¯le *IntReg*. Its temperature is 120^0C, and it has the highest power density, 2.798 *Watt=mm*2. Usually the block with the highest power density has the highest temperature, but it is not always true. The temperature of a block in a chip depends not only on its power density but also on the power density of the adjacent blocks. We can take blocks *IntQ* and *FPReg* as an example. The power density of *IntQ* is 0.137 *Watt=mm*2, and the power density of *FPReg* is 0.623 *Watt=mm*2, which is nearly 4 times larger than that of *IntQ*. However, the temperature of *IntQ* (85.3^0C) is higher by about 9^0C than the temperature of *FPReg* (76.5^0C). This is because *IntQ* is placed near the blocks *IntReg*, *LdStQ*, and *IntExec*, all of which are hot blocks. In contrast, *FPReg* is placed near *FPMul*, *FPAdd*, both of which have relatively low power densities. This demonstrates that the placement of a block has a considerable impact on its temperature.

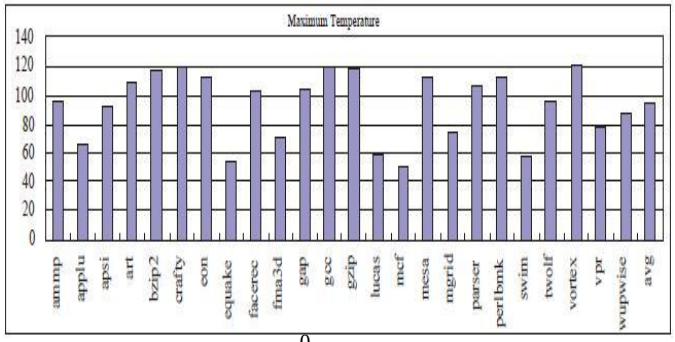

Fig-6: Maximum temperature (^{0}C) for the original alpha floorplan for SPEC2000 benchmarks.

The maximum temperature for SPEC2000 benchmarks in is shown in Figure 6. We can see that for 12 out of the 24 benchmark the maximum temperature of the chip is higher than 100^0C, for 8 of them the temperature exceeds 110^0C, and for 2 of them it exceeds 120^0C. When we take a look at the hottest block in the chip, we find that it is *IntReg* for almost all SPEC2000 benchmarks expect for *applu*, *lucas*, and *mgrid*. *FPReg* is the hottest block for *applu* and *FPAdd* is the hottest block for *lucas* and *mgrid*. owever, their maximum temperatures are not high (67.2^0C, 59.1^0C and 75^0C, respectively) [10]. Since the temperature distribution among the blocks of the chip for SPEC benchmarks is similar, we select as the representative benchmark in our experiments the *gcc* benchmark, which has a maximum temperature of 120^0C.

V. RESULTS AND DISCUSSIONS

The simulated annealing and B*Tree hybrid floor planning algorithm is implemented in C programming language on a Intel® Pentium® CPU 2020M @ 2.40 GHz PC. The alpha benchmark circuit has been used that consist of hard modules. We tested these benchmarks Table-1; give the temperature of alpha benchmark. Since the benchmark contains modules with fixed dimensions, we adopt a procedure to convert fixed dimension into variable dimension. We adopt a procedure to convert fixed dimension into variable dimension for our floor planning algorithm. We calculated the original temperature of alpha benchmark circuits. In the simulated annealing process the temperature was decrease at constant rate (0.9).

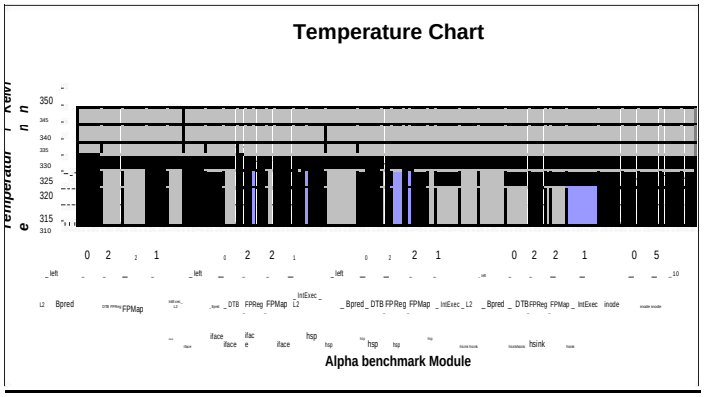

Figure-7: Temperature Chart of Alpha Benchmark Module

We first developed the simulated annealing floor planning algorithm based on B*Tree representation technique and used B*Tree representation for our floor planning algorithm as it is easy to implement has a smaller solution space and time complexity and many other advantage and then run algorithm on hotspot temperature simulator to check the result.

The simulation was conducted using 13µm alpha benchmark, one for each cost function for each function module. The results from each simulation are providing in Table-1, furthermore thermal maps have been provide for alpha benchmark. The result shows significant decrease in temperature and also decrease in area, width and height as well as reliability has improved. The function modules L2 decrease from 323.86^0K to 323.23^0K, L2_right decrease from 324.68^0K to 323.79^0K, Icache decrease from 331.09^0K to 330.04^0K, Bpred decrease from 333.99^0K to 327.67^0K, DTB decrease from 328.61^0K to 324.56^0K, FPAdd 329.41^0K to 326.48^0K, FPReg 329.29^0K to 325.46^0K, FPMul 328.18^0K to 326.54^0K, InQ 328.51^0K to 327.59^0K, IntReg 344.01^0K to

332.45^{0}K, IntExec 335.45^{0}K to 334.62^{0}K, FPQ 327.86^{0}K to 325.32^{0}K, ITB 330.37^{0}K to 325.99^{0}K and 9 different function modules merge into one module reduce the size and area of chip. The result shows average temperature decrease is 28.23%, total width and height reduce is 0.625% and total area reduce is 1.1328%.

Table-1 Result Hotspot tool

Before simulation Alpha benchmark				After simulation Alpha benchmark			
Unit Name	Temperature in Kelvin	Total Area in M^2	Total width and height in M	Unit Name	Temperature in Kelvin	Total Area in M^2	Total width and height in M
L2	323.86	0.0002560	0.01600	L2	323.23	0.00025311	0.01590
L2_right	324.68			L2_right	323.79		
L2_left	324.35			L2_left	323.88		
Icache	331.09			Icache	330.04		
Dcache	335.79			Dcache	335.79		
Bpred_0	333.77			Bpred	327.67		
Bpred_1	334.2						
Bpred_2	334.02						
DTB_0	328.8			DTB	324.56		
DTB_1	328.68						
DTB_2	328.36						
FPAdd_0	329.27			FPAdd	326.48		
FPAdd_1	329.55						
FPReg_0	329.11			FPReg	325.46		
FPReg_1	329.32						
FPReg_2	329.54						
FPReg_3	329.45						
FPMul_0	327.97			FPMul	326.54		
FPMul_1	328.39						
FPMap_0	325.47			FPMap	327.12		
FPMap_1	326.01						
IntMap	329.29			IntMap	330.02		
IntQ	328.51			IntQ	327.59		
IntReg_0	343.73			IntReg	332.45		
IntReg_1	344.29						
IntExec	335.45			IntExec	334.62		
FPQ	327.86			FPQ	325.32		
LdStQ	337.5			LdStQ	337.9		
ITB_1	330.68			ITB	325.99		
ITB_0	330.07						

VI. CONCLUSION

3D-ICs technologies circuits and layers are implemented. An algorithm was developed at the floor planning stage which takes into account the performance degradation in thermal dissipation. We have shown how to improve the temperature distribution of a chip and reduce hotspots. We have also demonstrated that the peak temperature can be reduced up to 3.43% that is 344.29^{o}K to 332.45^{o}K. Also an average temperature of Alpha benchmark decrease up to 28.23% and even reducing the size up to 0.625% and area reducing up to 1.1328%.

As design uncertainty affects the power and temperature of the chip besides the timing of circuits considerably, we need to predict the ranges of these parameters as well, under the presence of variations in dimensions of modules. This work can be extended to estimate the range of power dissipation for each functional block by taking into account the range of its area. Similarly, range of power dissipation of each interconnect can be determined by taking into account the range of its net length. So, it provides a promising framework for significant future work in the direction of computing

impacts of design uncertainty on power dissipation and emperature estimations of the chip at the floor planning stage.

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