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Edge Encoding Technique for Reducing Noise and Power Consumption in a PLL

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***Abstract*— This paper proposes a new reference spur elimination architecture for a charge pump PLL using an edge encoding technique. This uses the dual edge triggered flip flop and shifts the rising and falling edge by different amounts. This paper proposes two schemes to reduce the initial frequency and power in a PLL. The prototype PLL was fully integrated in a 0.18-m CMOS technology.**

Index terms- Edge encoder, phase locked loop, spur.

I. INTRODUCTION

A. PHASE LOCKED LOOP

Periodic disturbance on the input of the voltage-controlled oscillator (VCO) that is due to the charge-pump (CP) current mismatch and leakage causes the large reference-spur in a CP-based phase locked loop (PLL) output spectrum. In RF systems, this reference spur and its harmonics are mixed with various interferers, which results in degradation of the overall system performance. Moreover, as modern communication systems increasingly require covering wide frequency bands, reference-spur-related issues become more critical.

Recently, a great deal of effort has been made to develop techniques and methods to reduce the reference spur level. One common approach is to decrease the loop-bandwidth of a PLL. However, a narrow loop-bandwidth increases the settling time or restricts the data rate when the PLL is used as a direct modulator. Another solution is to adopt a higher-order loop filter, but if the loop and width is not much smaller than the reference frequency, the fundamental spur cannot be sufficiently suppressed. What's more, the complex loop-characteristic with additional poles may cause the closed loop to be unstable. Alternatively, the frequency-voltage gain of a VCO, K_{VCO}, can be reduced to alleviate the effect of the frequency/phase modulation of a VCO control voltage. Because a reduced K_{VOC} limits the frequency-tuning range, the PLL should consider a tuning-range compensation technique, such as the switched capacitor (SC) technique or the dual-path-controlled VCO technique. However, the SC technique with a small K_{VOC} must equip a complicated digital- band-selection algorithm for extending the tuning range, and the band-selection algorithm requires an additional frequency selection time even before the PLL starts the frequency-acquisition process.

On the other hand, the dual-path-controlled VCO technique raises the tradeoff between phase noise and a frequency-tuning range.

A number of coding techniques including encode the conventional bus such that adjacent bits never switch in the opposite direction. However, in addition to the special encoder and decoder circuit overhead, these techniques require additional wires for bus encoding which increase routing area. It is not clear whether the conventional bus could better use extra spacing at the same footprint instead of additional wires for better speed and energy consumption

II. EXISTING WORK

Jaehyouk Choi, Kyutae Lim, Woonyun Kim [1] proposes the edge interpolator for a CP-based PLL to eliminate the reference spur and its harmonics through the charge-distribution mechanism. Thus, in the PLL that adopts the proposed edge interpolator, the process delivering the phase/frequency difference information between the reference clock signal f_{ref} and the divided signal f_{div} from the PFD/CP to the VCO is distributed into *k* consecutive times. Fig. 1 presents the relationship between disturbance of the VCO control voltage and the reference spur in the output spectrum, both in a conventional PLL and in the PLL that adopts the proposed edge interpolator. In a conventional PLL where N=1, one strong disturbance of the control voltage of the VCO occurs in every reference period. However, in the PLL with the proposed technique, where N=*k*,*k* consecutive small disturbances modulate the VCO. Therefore, instead of the original reference spur and its harmonics, the new fundamental reference spur appears at *k*-times higher frequency, and the spur-free frequency band is extended.
To guarantee the functionality of the edge interpolator in implementation, two critical issues should be addressed: every new edge in the f_{ref_int} should be placed at regular intervals of T_{ref}/k, and every corresponding pair of interpolated edges in the f_{ref_int} and the f_{div_int} has to maintain the same phase difference as that of the original edges in the f_{ref} and the f_{div} to deliver the phase difference information to the VCO accurately through the PFD/CP.

Fig. 1 details the operation of the edge generator and the edge combiner. When the phase-shifted signal from the VCDL Φ_1 enters the corresponding *l*th DFF Q_1 becomes high if the value in the D node is set high. In the meantime, Qb1 becomes low and resets Q_1 by triggering the RSTb node. Since this reset process takes two inverter delay times, a pulse of short duration is generated at Q_1. Finally, the subsequent edge combiner collects these pulses.

To ensure that the phase difference between every corresponding pair of edges of the f_{ref_int} and the f_{div_int} equals that between the original edges of the f_{ref} and the f_{div}, the VCDLs were interleaved as one group in the layout.

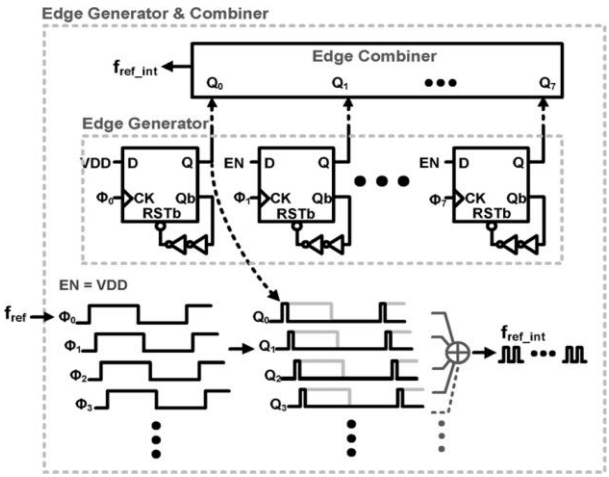

Fig 1: Edge Generator and Combiner

III. PROPOSED WORK

A. Objectives

The objective of the edge encoder is to selectively shift the rising and falling transition by different amounts. This encoding is done simply by performing an AND operation between the original signal and the half-cycle delayed version of itself. In this way, only the rising edge is delayed by a half cycle, separating simultaneous rising and falling transition by a half cycle. Since the encoder logic is very simple, the encoding overhead in terms of power and area is very small. This makes the edge encoding technique a highly practical approach.

B. Overview of the proposed Work

This paper presents a new encoding technique that is done by controlling the edges of rising and falling transition in time, namely always performing rising transitions on the negative edge of the clock and falling transition on the positive edge of the clock (or vice versa). Since the worst-case switching is separated by as much as one phase (half clock cycle), this technique remains robust against process variation. Hence, both the average and worst-case energy can be reduced without impacting the sensitivity to process variation.

IV. EDGE ENCODING SCHEME

There are two schemes to effectively use the edge-encoding technique. The two methods differ in the procedure to cope with the initial half cycle latency required for edge encoding and to address the issue of aligning back to the positive-edge triggered signal at the far end of the wire.

A.ZERO LATENCY SCHEME:

When data toggles every cycle, the encoder generates a half-cycle pulse (enc_out). As this half-cycle pulse propagates through an even number of dual-edge flip-flops, it automatically aligns back to a positive edge triggered signal (ff4_out) at the far end. Therefore, there is no need for any decoder circuit. The one-cycle latency is therefore introduced once at the beginning of the wire and the throughput is not hampered. After the encoding, the data must eventually align to the positive edge of the clock at the far end of the wire. To achieve this, we can align the transition at the near end to the positive edge of the clock by encoding with a full one cycle delay, and then allow for normal signal.

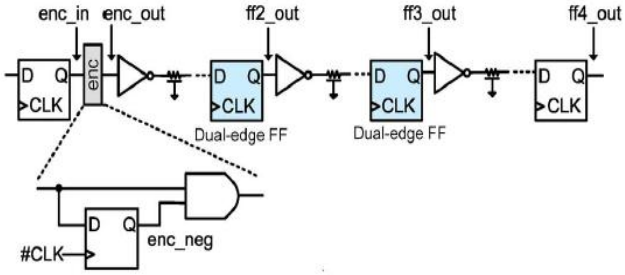

Fig 2 Edge Encoder Logic Diagram

B.ONE CYCLE LATENCY (OCL) SCHEME:

The difference in the encoder compared to ZL is that a dual-edge flip-flop is added at the output to intentionally delay enc_in by one cycle and align the rising edge of enc_out at the positive edge of the clock. Since the edge encoding technique requires dual-edge flip-flops, the number of flip-flops placed is inevitably increased compared to single-edge flip-flops. First, due to shorter distance between dual-edge flip-flops, the slew rate constraint in the edge encoding scheme should be morestringent the proposed schemes include more flip-flops it is worthwhile to investigate the impact on static power.

C.DUAL EDGE FLIP FLOP:

Since the edge encoding technique requires dual-edge flip-flops, the number of flip-flop is increased compared to single-edge flip-flops. First, due to shorter distance between dual-edge flip-flops, the slew rate constraint in the edge encoding scheme should be more stringent. Both in the

conventional and edge encoding schemes, the repeaters between flip-flops are sized such that 10%–90% slew rate is 10% of the respective signal propagation delay between the flip-flops.

V. PERFORMANCE EVALUATION

A. Simulation Model and Parameters

We use cadence tool to simulate our proposed algorithm. In this project, simulation is done with the help of cadence nclaunch digital simulation tool. Following comments are used for compilation and elaboration of the design.

Cadence digital lab tools:

ncvlog: Compiles Verilog files

ncelab: Elaborates the design and generates a simulation snapshot

ncsim: Simulates the snapshot

Simulation results and parameters are summarized in table 1.

TABLE I

	Power	Frequency	Current
ZL	145Mw	171.5MHz	15mA
OCL	153mW	195MHz	16.5mA

B. Results

The results for edge encoding in a pll is given below.

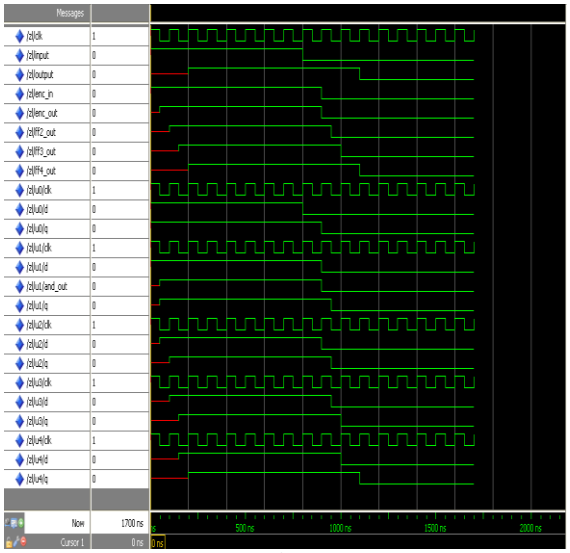

Figure 1. Simulation of Encoder in ZL Scheme

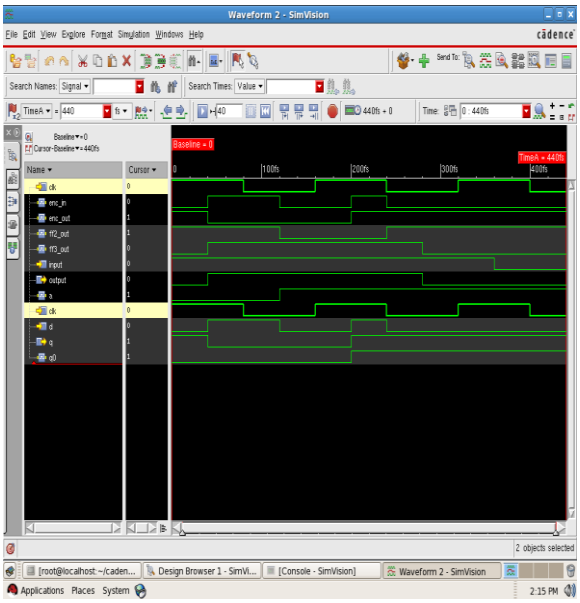

Figure 2. Simulation of OCL Scheme

Figure 1 show the results edge encoding for zero latency in a charge pump pll for equal the delay and reducing the leakage current.

Figure 2 shows the results edge encoding for one cycle latency scheme in a pll.

VI. CONCLUSION

In this paper, we proposed two new edge encoding techniques to reduce the power consumption and to reduce the initial frequency in PLL. Since the proposed architecture utilized only one PFD/CP pair and the edge encoding based dual edge flip flop, it effectively embodied the theoretical idea without unequal delay intervals and mismatches. In this ZL scheme is better than the OCL scheme.

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