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Development of CMOS-Based Dual Mode Logic Gates

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***Abstract*-The dual mode logic is an efficient model, which is having static and dynamic mode of operation. The static mode gives very low power dissipation but speed is very slow. The dynamic mode gives high performance. A basic DML gate is very simple and is composed of any static logic family gate and an additional clocked transistor. We introduce the logical effort (LE) methodology for the CMOS-Based DML family. The proposed methodology used to power reduction, delay optimization of DML logic. This is done by the development of complete and approximated LE models, which allows easy extraction of design optimization parameters, such as gate sizing factors and delay estimations.**

Index Terms- Dual Mode Logic, Logical Effort, Low Power, Optimization

I. INTRODUCTION

Logic optimization and timing estimations are basic tasks for digital circuit designers. The logical effort (LE) method was first presented by Sutherland *et al* for easy and fast evaluation and optimization of delay in CMOS logic paths. Because of its elegance, the LE method has become a very popular tool for designing and education purposes and is adopted to be the basis for several computer-aided-design tools. Although LE is mainly used for standard CMOS logic, it is also shown to be useful for other logic families, such as the pass transistor logic. Here, in this paper we are using a well known model DML [1] which provides the designer a very high flexibility. As above mentioned DML [1] has overcome the disadvantages of the following two methods namely static mode and dynamic mode. Since, in static mode of operation the power dissipation is low and speed is also very low compared to the dynamic mode. Similarly in dynamic mode the speed is very high and power dissipation is also high compared with static mode. The objective of this paper is to design an improved in terms of Speed especially and an allowable power dissipation and also minimizing the delay. The rest of this paper is having: a review on the DML family explained in the section – II, and in the section –III contains all the implementation of proposed system. And section –IV contains the comparison with the ordinary normal and all the results in terms of power dissipations and delay. Section –V contains the conclusion on the work and future work on this proposal.

II. OVERVIEW OF DML FAMILY

A basic DML gate is having a normal static logic gate, which can be a conventional CMOS logic gate and at the output side we are connecting a normal transistor. And whose gate is connected to a global clock signal is applied to it as switching circuit. The whole operation is based upon this external connected transistor and its clock signal speed. The DML can be arranged as two ways depending upon the type of transistor using at the output side either PMOS or NMOS transistor as following way shown in the fig 1.

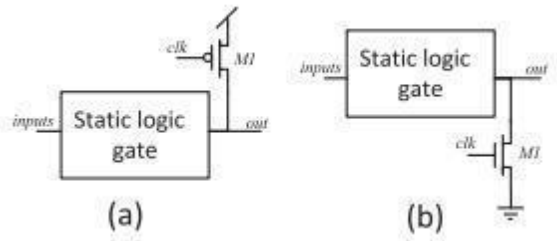

Fig 1: DML topology: (a) type A and (b) type B

As shown in above figure (a) PMOS is connected at the output side and clock is enabled high and similarly in figure (b) at the output side NMOS is connected and clock is enabled low for the switching operations. In above figure (a) when transistor M1 is enabled high the gate is operated in static mode and in figure (b) when transistor M2 is enabled low the gate is again works as normal static mode. But, when the transistor M1 is enabled with clock having both high and low modes then the gate acts as DML gate. Similarly in the type B transistors there is a much more efficiency when compared with an pull-up transistor in type A topology and similarly pull-down transistor in type B topology. Due to this a robust efficiency is achieved in these DML topologies. Here, the design is operated in two modes of operations based up on the clock signal i.e.

1) pre-charge and 2) evaluation modes.

III. RELATED WORKS

A new approach to technology mapping, based on the theory of logical effort. The improvement obtained by our algorithm due to the solution of load distribution problem, which allows for accurate assignment of capacitances at multiple fan-out points. This algorithm maps individual trees such that the solution of the entire circuit is optimal. In traditional technology mapping, the best match for a gate depends on the load being driven, which is not known at the matching stage. This paper addresses the problem of delays, load-dependent delay model, constant delay models. The logical effort method used to estimate the delays.

Technology mapping step of synthesis binds a technology independent logic level description of a circuit to a library of gates in the target technology. A number of algorithm used to tree mapping and DAG-mapping using load-dependent delay models, constant delay models, the logical effort method used to get high-performance in rich libraries. The problems of minimum-delay technology mapping apply the logical effort. The load-distribution problem, which occurs in the case of circuits with multiple fan outs. The cumulative path logical effort it is minimizing the cost in simple path with each gate having one fan in. In load distribution problem circuit with multiple fan outs and circuits collect the fan out free regions; the critical input of a fan out free region is not well defined. The circuit is initially divided into fan out free regions. The technology mapping using logical effort method used to get the minimum delay and optimal solutions.

Sub-threshold circuit designs demonstrated to be a successful alternative when ultra-low power consumption is paramount. However, the characteristics of MOS transistors in the sub-threshold region are significantly different from those in Strong inversion. This presents new challenges in design optimization, particularly in complex gates with stacks of transistors. The robustness of static CMOS logic can operate with supply voltages below the transistor threshold voltage. The low operating frequency and low supply voltage combine to reduce both dynamic and leakage power. The MOS saturation current, which was a near linear function of the gate and threshold voltages in the strong inversion region, becomes an exponential function of those values in the sub threshold region. A closed-form solution for the optimal sizing of stacked transistors is derived and shown to match experimental results. Finally, we present HSPICE simulation results from ISCAS benchmarks and component circuits demonstrating the advantage of our approach versus the conventional logical effort method.

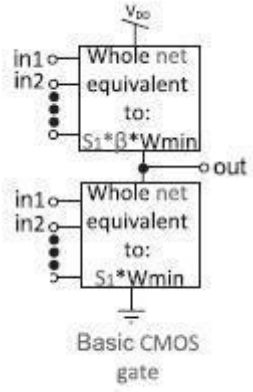

Fig.2 Standard CMOS gate with sizing factors

The input and output capacitances of the DML gates are significantly reduced, as compared with CMOS gates, due to the utilization of minimal width transistors in the pull-up of Type 1 or pull-down in Type *B* networks. The size of the precharge transistor is kept equal *S***W*min to maintain a fast precharge period despite the increase in the output load. Contrary to CMOS gates, each DML gate can be implemented in two ways, only one of which is efficient. The preferred topology is such that the precharge transistor is placed in parallel to the

stacked transistors, i.e., NOR in Type *A* is preferred over NAND, and NAND in Type *B* is preferred over NOR. In this case, the evaluation is performed through the parallel transistors and therefore it is faster. As presented the optimal design methodology of DML gates is to serially connect Type *A* and Type *B* gates, similarly to np-CMOS/NORA techniques. Even though this design methodology allows maximum performance, area minimization and improved power efficiency, serial connection of the same type gates is also possible. However, this case presents many drawbacks, such as the need of footer/header and severe glitching. These well-explored problems are standard for dynamic gates design. DML strength is that static mode CMOS-based DML gates with transistor sizes optimized for the dynamic mode is actually a semi energy optimal CMOS construction of a gate because of reduced static and switching energy consumption. The static operation of the DML gates is used to significantly reduce energy consumption in performance. A general approach is to optimize the delay for the dynamic mode of operation and operate the system in the static mode only in standby/low-energy mode without severe frequency restrictions in performance is reasonable.

IV. PROPOSED SYSTEM

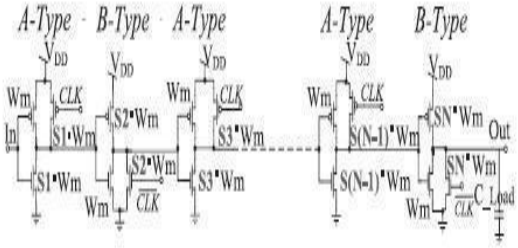

Fig3. DML NOR chain with sizing factors

Complete Unapproximated (CS) Method for the Sizing Factors of DML NOR gate Chain

This is method most optimal and accurate solution for DML NOR chain sizing. However, solving it is a very exhausting task. This unapproximated solution (CS) is much more complex than a simple CMOS LE optimal solution, which is derived with no assumptions and approximations.DML CS method complexity is due to a nonstandard sizing of transistors, connected in parallel to the Clocked transistor. In this methodology I use proper size of the entire transistor. The NOR gate chain is used to analyse the power and delays. Here I use 20 number of NOR gates and all transistors width and length same size.

Complete Approximated (CA) Method for the Sizing Factors of DML NOR Chain

To reduce the complexity of the LE method, a CA solution, which trades off the complexity and accuracy, is developed. The CA method assumes that the contribution of minimal transistors to the drain and gate capacitances is negligible for all stages of the chain. In this methodology I use all transistors are different sizes. Here the NOR chain use all gates different size transistors. This methodology consumes more power and also delay is high.

SA Method for the Sizing Factors of DML NOR Chain

In this methodology I use half of the transistors gate sizes are same another half of the transistors gate sizes are same. Here two types of the gate sizes are used to analyse the power and delay. This consumes moderate power and delay.

COMPARISON OF CS, CA, SA METHODS

Method	Maximum Power Consumption	Average Power Consumption	Minimum Delay
Complete unapproximated	1.022045e-006 watts	6.251566e-007 watts	2.2571e-007ns
Complete approximated	8.600728e-006 watts	4.539475e-007 watts	2.3353e-007ns
Semi approximated	7.747827e-006 watts	4.388112e-007 watts	2.2547e-007ns

Table.1 Comparison of CS, CA, SA Methods

Following fig 2 shows the proposed efficient DML complete unapproximated method which can be used in a situation where the systems need a faster operation, delay and the power dissipations are considered up to some extents.

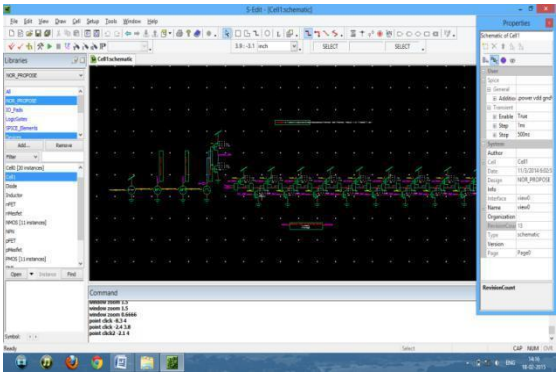

Fig4.UNAPPROXIMATE METHOD

The above showed figure is the symbol based DML unapproximate which is designed in the Tanner Platform by creating symbols to each and every design. For each and every gate at the output side a PMOS gate which is works as an Pull-up circuit in the design, and NMOS gate which is works as an pull-down circuit.

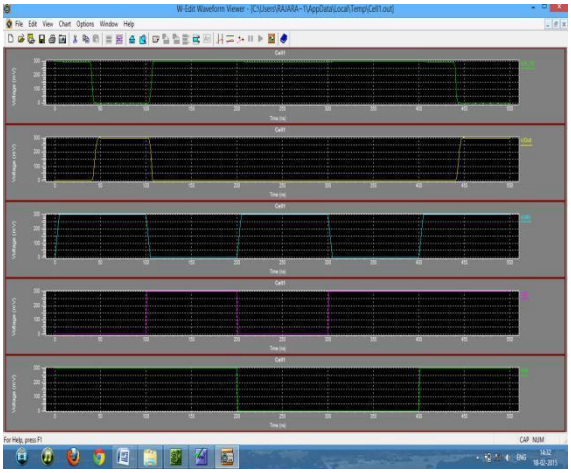

Fig.5 Schematic of Unapproximated NOR chain

V. CONCLUSION

A novel LE approach for CMOS-based DML logic network is presented. The proposed approach is given maximum performance in the dynamic mode of operation. This paper presented three different approaches. The first approach is complete unapproximated method in that all the transistors are proper gate sizing in the DML inverter chain. The second approach is complete approximated in that all the transistors are of different gate sizing in the DML inverter chain. The third approach is semi-approximated in that two different sizes of gates are used in the DML inverter chain. The complete un approximated method is consume less power compared to other two methods and this method has minimum delay performance.

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