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Design of Explicit Pulse Triggered Flip-Flop for Low Power Applications

R.Gowri,
PGScholar /Department of ECE,
Anna University Regional Office, Madurai, India

Mr.A.Muthukrishnan,
Assistant Professor/Department of ECE,
Anna University Regional Office, Madurai, India

***Abstract*—In this paper, a low power pulse triggered flip-flops are designed. P-FFs are more popular than the conventional transmission gate (TG) and master–slave based FFs because it contains single latch structure. Pulse triggered flip flop in terms of pulse generation can be classified as implicit and explicit pulse triggered flip flop.The explicit pulse triggered flip flop is more advantage than implicit pulse triggered flip flop. Several flip flops like conditional capture, conditional discharge, and conditional pulse enhancement flip flop are designed but they have longer delay, area and consume more power. In this modified signal feed through scheme flip-flop and flip-flop with modified pulse generator circuit are proposed. These proposed designs solve longer delay, improve the speed of the data transition and achieves better power performance.**

Based on layout simulation results using TANNER EDA 250-nm technology, the proposed design outperforms the conventional P-FF design by using only 17 transistors.

Index Terms-Flip-flop (FF), low power, pulse-triggered.

I. INTRODUCTION

The clock system composed of the clock interconnection network and timing elements (flip-flops and latches) is one of the most power consuming components in a very large scale integration (VLSI) system. It accounts for 30%–60% of the total power dissipation in a system [3]. Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. The digital designs now a-days often adopt intensive pipelining techniques and employ many FF-rich modules such as shift register, and first in-first out. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design.

Pulse-triggered FF (P-FF) is more popular than the conventional transmission gate (TG) and master–slave based FFs inhigh-speed applications [4]-[7].Traditional master-slave flip-flops consist of two stages, master and slave and they are characterized by hard-edge property. Hard-edged flip-flops are characterized by positive setup time, causing large -to- delays.Alternatively, pulse-triggered flip-flops consist of only one stage and are characterized by the soft edge property. The circuit complexity and number of stages inside these pulse-triggered flip-flops are reduced, leading to small -to- delays. This circuit simplicity lowers the power consumption of the clock tree system.

A Pulse triggered flip-flop consists of a pulse generator for generating strobe signals and a latch for data storage. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. To obtain the balanced performance among power, area and delay, design space exploration is also a widely used technique.

Depending on the method of pulse generation, Pulse triggered flip-flop designs can be classified as implicit or explicit [8]. In an implicit P-FF, the pulse generator is a built-in logic of the latch design hence no explicit pulse signals are generated. In an explicit P-FF, the designs of pulse generator and latch are separate [9]. Without generating pulse signals explicitly, implicit P-FFs are in general more power-economical and they suffer from a longer discharging path, which causes inferior timing characteristics. Explicit pulse generation incurs more power consumption but the logic separation from the latch design gives the flip-flop design a unique speed advantage. Its circuit complexity and power consumption can be effectively reduced if one pulse generator shares a group of FFs (e.g., an n-bit register).

The rest of the paper organizes as follows: Section II explains briefly about the related work papers. Section III explains about the existing pulse triggered flip-flop.Section IV explains about objective of proposed pulse triggered flip-flops. Section V shows the comparison result for existing and proposed flip-flops. Section V concludes this paper and gives directions for future research.

II. RELATED WORK

Jin-Fa Linhas [1] has designed a pulse triggered flip-flop based on signal feed through scheme .The flip-flop

consists of pulse generator and modified true single phase clock latch. This method is used to solve long discharging path problem inconventional explicit type pulse-triggered FF by using simple pass transistor and shorten the longer delay to achieve better speed and power performance. In this flip-flop leakage power is increased.

Hwang Y.T, Lin J.F, and Sheu M.H have designedpulse triggered flip-flop based on Conditional pulse enhancement scheme [2].In the pulse generation control logic a simple two transistor AND gate design is used to reduce the circuit complexity. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. The proposed design features the best power-delay-product performance compared with the conventional transmission gate-based FF design and the average leakage power consumption is also reduced.

MyintWaiPhyu, Kangkang Fu, Wang Ling Goh,Kiat-Seng Yeo suggesta new technique for implementing low-energy double-edge triggered flip-flops based on a clock branch-sharing scheme to reduce the number of clocked transistors in the design [15]. The newly proposed design also employs conditional discharge and split-path techniques to further reduce switching activity and short-circuit currents respectively. The proposed CBS_ip design has an improvement in view of power consumption and PDP. But the clock branch sharing structure is more complicated.

Chen Kong Teh, MototsuguHamada,TetsuyaFujita,Hiroyuki Hara,and YukihitoOowakihave designed low-power and high-performance flip-flops, namely conditional data mapping flipflops[19].It reduces their dynamic power by mapping their inputs to a configuration that eliminates redundant internal transitions. In this Conditional data mapping flip-flop with differential and single-ended structures are designed.CDMFFs havethe best internal race Immunity among pulse-triggered flip-flops.

B. Kong, S. Kim, and Y. Jun have designed a family of novel low-power flip-flops, called conditional-capture flip-flops (CCFF) based on Conditional capture technique[16]. They achieved statistical power reduction by eliminating redundant transitions of internal nodes. These flip-flops have negative setuptime and they provide small data-to-output latency and overcoming clock skew-related cycle time loss.The proposed single-ended structure provides power comparable to the fully static master–slave design with significantly reduced data-to-output latency.

P. Zhao, T. Darwish, and M. Bayoumi have designed high-performance flip-flops based on the conditional precharge and the conditional capture technologies [18]. These techniques are used to prevent or reduce the redundant internal switching activities. This CDFF not only reduces the internal switching activities, but also generates less glitch at the output, while they maintain the negative setup time and small D -to- Q delay characteristics.

III. EXISTING FLIP-FLOP

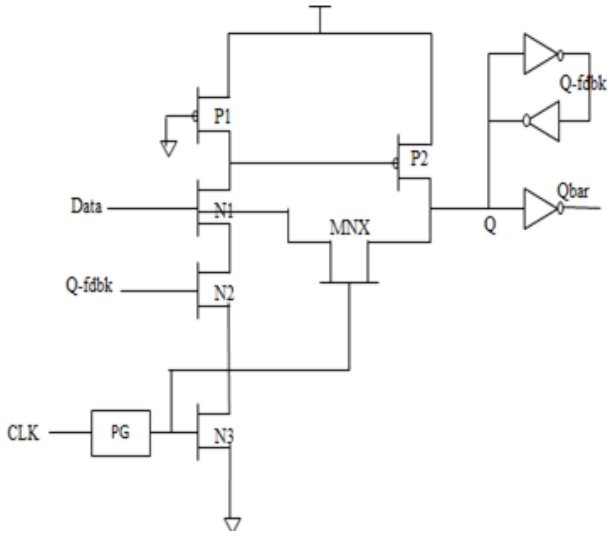


Fig: 1Existing Pulse Triggered Flip-flop

Figure shows the existing pulse triggered flip-flop, a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of pass transistor and pseudo NMOS logic. The idea is to provide a signal feed through from input source to the internal node of the latch, which facilitates extra driving to shorten the transition time.

Similar to the SCDFF design, the PFF design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. First, a weak pull-up transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This result in pseudo-nMOS logic style and the charge keeper circuit for the internal node Xcan be stored. Second, a pass transistor MNx controlled by the pulse clock is included .So that input data can drive node Q of the latch directly. Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, it facilitates auxiliary signal driving from the input source to node Q.When a clock pulse arrives, if no data transition occurs the input data and node Q are at the same level and current passes through the pass transistor MNxwhich keeps the input stage of the FF from any driving effort. At the time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down path of node Xis off. On the other hand, if a “0” to “1” data transition occurs, then node Xis discharged to turn on transistor MP2 then node Q will be large. The drawback of this flip flop is high power consumption and large area.

IV. OBJECTIVES & OVERVIEW OF THE PROPOSED WORK

The objective is to reduce the power, delay, area and improve the speed of the data transition in pulse

triggered flip-flop. A pulse triggered latch is also a two stage flip-flop where the first stage is a pulse generator and the second stage is a latch. Race conditions are thus avoided by keeping the transparent period of the latch very short.

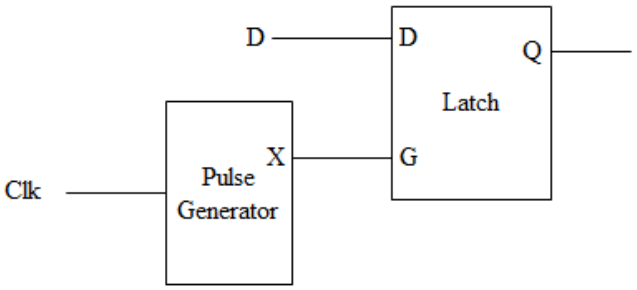


Fig: 2 Block Diagram of Pulse Triggered Flip-Flop

In pulse triggered flip flops only one latch is used whereas it is two in normal edge triggered flip-flops. Ashort pulse around every rising or falling edge of the clock is created through a pulse generator circuit. This generated pulse acts as the clock input to a latch.

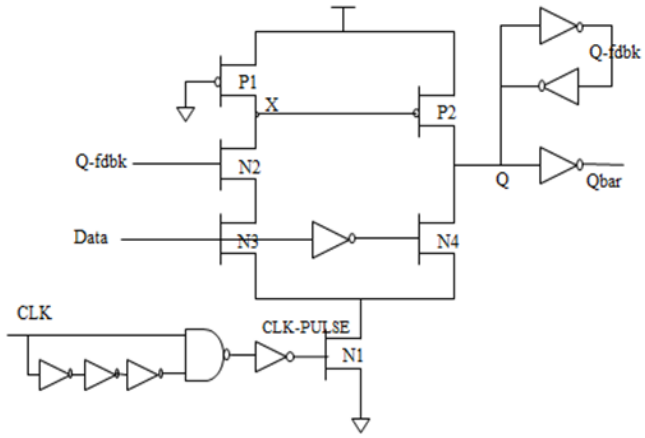
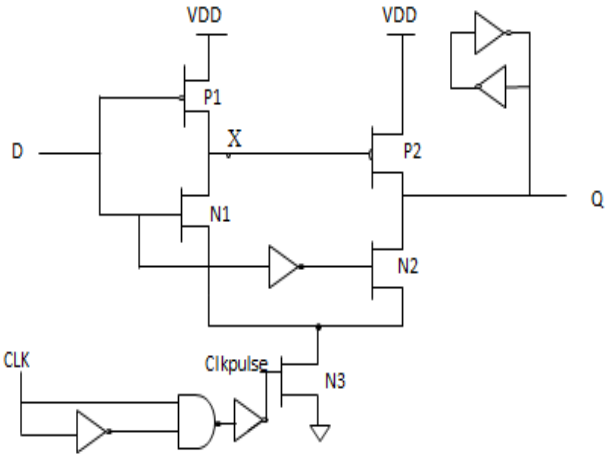


Fig: 3 Proposed P-FF1 design

When clock pulse is enabled the transistor N1 is ON and Data is propagated to output.PMOS transistor P1, whose input is continuously grounded. Hence node X will be high most of the time. The evaluation path transistor N2 is controlled by the feedback from the output (q- fdbk). Using Pseudo NMOS (always on PMOS P1) takes advantage of the fact that D and Q bar have inversed polarity resulting from the conditional discharge technique. In this the clock is converted into clk pulse by pulse generator. The discharging path only stays ON for a short time yielding a little short circuit current. An inverter is placed after Q is used for providing protection from unwanted noise coupling. When CLK rises, CLK-Pulse will stay high for a short time interval .During this period, the clocked transistor N1 turns on. The first stage in the design is responsible for capturing 0->1input transitions of D. The internal node X will discharge causing the outputs Q and Q bar to be HIGH and LOW, respectively. N2 turns off by Q_fdbk=0. If the input D stays "1," the first stage is disconnected from ground. The second stage, on the other hand, is responsible for capturing the input transitions. If the input D stays "0", the second stage is disconnected and first stage is responsible for capturing the input transitions.

Fig: 4 Proposed P-FF2 design



The proposed flip flop consists of two cascaded static latches sharing one clocked transistor shown in fig. The internal node X is asserted or disserted according to the input data D during the transparent interval. The internal nodes of flip flop switch only when input changes. At the rising edge of the clock, transistorN3turns on for a short time interval and the circuit acts like two cascaded inverter allowing the input data to propagate to the output. After this short time interval, N3 switches off, causing the NMOS stacks of both stages to be disconnected from the ground supply, preventing the propagation of the input to the output. The output state Q is maintained by the keeper. In this pulse generator circuit is modified, the number of inverter stage is reduced. If the input data is "1" then the node X becomes "0" which turn ON P2 transistor and Q becomes "1". If the input data is "0" then the node X becomes "1" which turn OFF P2 transistor and Q becomes "0". In this proposed design the number of transistor count is reduced hence area and power is also reduced.

V. RESULTS

The target Technology is TSMC 250-nm CMOS Process. The supply voltage is 3V. The setup used in our simulations is shown in Fig 5.

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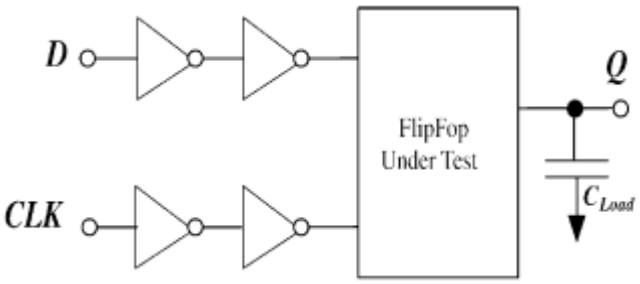

Fig: 5 Setup used for the flip-flops simulations

The flip-flops' inputs (clock, data) are driven by fixed input buffers, the outputs are required to drive an output load.Since the proposed design requires direct output driving from the input source. For comparisons of the power consumption of the data input buffer (an inverter) is included. The output of the FF is loaded with 18-fF capacitor. The load capacitance of 3 fF is also placed at the output of the clock buffer.

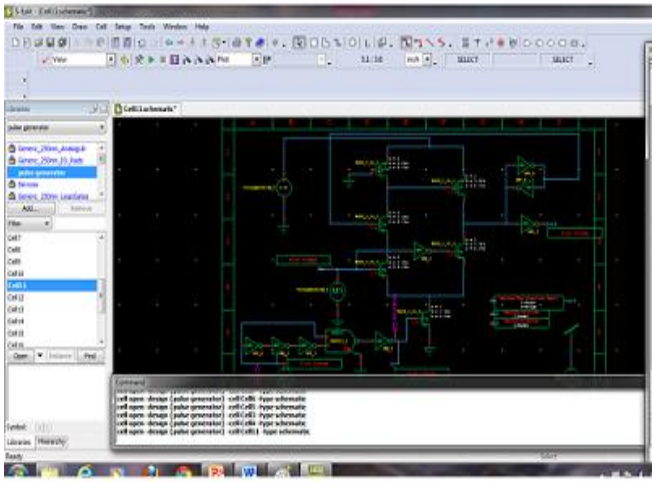

Fig: 6 Schematic view of Proposed Flipflop1

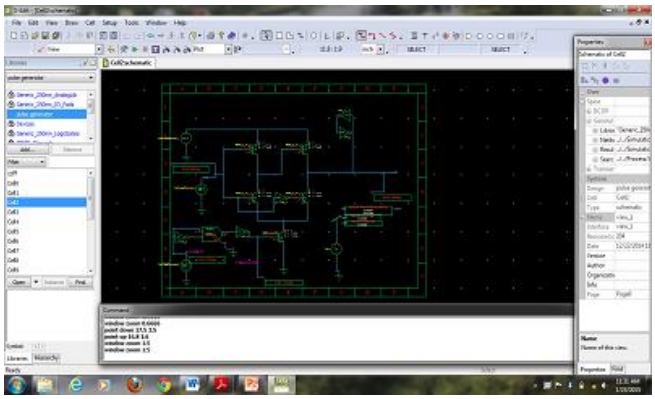

Fig: 7 Schematic view of Proposed Flipflop2

Table.1. Comparison of various P-FF designs

P-FF(Pulse triggered flip-flop)	Existing FF	Proposed FF1	Proposed FF2
Power(mW)	6.67	2.5	2.5
Delay(ns)	4.5855	4.6926	2.7013
No of Transistors	24	26	19

VI. CONCLUSION

A new proposed pulse triggered flip flops are designed which show better performance as compared to other existing flip flop. The P-FF consists of pseudo NMOS logic. These designs are simulated in Tanner tool and the results and waveforms are also obtained. The power of proposed designs is comparatively lesser than other existing flip flop and also the delay of the flip flops are reduced. The explicit pulse triggered flip flop shows better performance than implicit pulse triggered flip flop because if group of flip flop is used only one pulse generator is needed hence the power and area is reduced. These Pulse triggered flip flops can be used for the design of counters and shift registers.

REFERENCES

[1] Jin-Fa Lin, "Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme," *IEEE Trans. Very Large Scale Integr. (VLSI)Syst.,* vol. 22, no.1, Jan.2014.

[2] Y.-T. Hwang, J.-F. Lin, and M.-H. Sheu, "Low power pulse triggered Flip-flop design with conditional pulse enhancement scheme," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 2, pp. 361–366, Feb. 2012.

[3] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 807–811, May 1998.

[4] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high speed sense-amplifier-based flip-flop," *IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst.*, vol. 13, no. 11, pp. 1266–1274, Nov. 2005.

[5] H. Partovi, R. Burd, U. Salim, F.Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *IEEE Tech. Dig. ISSCC*, 1996, pp. 138–139.

[6] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R.Wang, A. Mehta, R. Heald, and G.Yee, "A new family of semi-dynamic and dynamic flip flops with embedded logic for high-performance processors," *IEEE J.Solid-State Circuits*, vol. 34, no. 5, pp. 712–716, May 1999.

[7] S. D. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. J. Sullivan, and T. Grutkowski, "The implementation of the Itanium 2 microprocessor," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1448–1460, Nov. 2002.

[8] V. Stojanovic and V. Oklobdzija, "Comparative analysis of master slave latches and flip-flops for high-performance and low-power systems," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[9] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in *Proc. ISPLED*, 2001, pp. 207–212.

[10] S. D. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. J.Sullivan, and T. Grutkowski, "The implementation of the Itanium 2 microprocessor," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1448–1460, Nov. 2002.

[11] S. Sadrossadat, H. Mostafa, and M. Anis, "Statistical design framework of sub-micron flip-flop circuits considering die-to-die and within-die variations," *IEEE Trans. Semicond. Manuf.*, vol. 24, no. 2, pp. 69–79,Feb. 2011.

[12] M. Alioto, E. Consoli, and G. Palumbo, "General strategies to design nanometer flip-flops in the energy-delay space," *IEEE Trans. CircuitsSyst.*, vol. 57, no. 7, pp. 1583–1596, Jul. 2010.

[13] M. Alioto, E. Consoli, and G. Palumbo, "Flip-flop energy/performance versus Clock Slope and impact on the clock network design," *IEEETrans. Circuits Syst.*, vol. 57, no. 6, pp. 1273–1286, Jun. 2010.

[14] M. Alioto, E. Consoli, and G. Palumbo, "Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: Part I - methodology and design strategies," *IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst.*, vol. 19, no. 5, pp. 725–736, May 2011.

[15] MyintWaiPhyu, Kangkang Fu, Wang Ling Goh,Kiat-SengYeo,"Power-Efficient Explicit-Pulsed Dual-Edge Triggered Sense-Amplifier Flip-Flops," IEEE Trans. Very Large Scale Integr. (VLSI) Syst, vol. 19, no. 1, pp.001-009, January-2011.

[16] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.

[17] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power-efficient dual-edge clocking," in *Proc. Int. Symp. Low Power Electron. Design*, Aug. 2002, pp. 56–59.

[18] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low power conditional discharge flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 477–484.

[19] Chen Kong Teh, MototsuguHamada,TetsuyaFujita,HiroyukiHara,NobuyukiIkumi,andYukihitoOowaki, "Conditional Data Mapping Flip-Flops for Low-Power and High-Performance Systems," IEEE Transaction Very Large Scale Integration system,vol. 14, no. 12, pp.1379-1383,December.2006.

Authors Profile

R.Gowri, received the **B.E.** degree in electronics and communication engineering from the P.S.R Engineering College, Sivakasi, Anna University, Chennai, India, in 2013. Currently doing **M.E.** in electronics and communication engineering (VLSI Design) in Anna University Regional Office, Madurai, India. Herresearch interest includes Digital Electronicsand Low Power VLSI Design.

A.Muthu Krishnan is working as a faculty in Electronics and communication Engineering in Regional Centre of Anna University Madurai. He completed his Bachelor degree in Anna University. He completed his Master's degree in VLSI Design in Anna University of Technology Coimbatore. He has five years of Teaching experience in Electronics and communication Engineering. Currently He is doing his PhD in Anna University, Chennai.His research interest includes wireless communication, Wireless Sensor Networks and VLSI Design.