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Designing High Performance Multi Port Router NoC With Shared Buffer

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Abstract- On-chip routers typically have buffers are used input or output ports for temporarily storing packets. The buffers are consuming some router area and power. The multiple queues in parallel as in VC router .While running a traffic trace, not all input ports have incoming packets needed to be transferred. Therefore large numbers of queues are empty and others are busy in the network. So the time consumption should be high for the high traffic. Therefore using a RoShaQ, minimize the buffer area and time .The RoShaQ architecture was send the input packets are travel through the shared queues at low traffic. At high load traffic the input packets are bypasses the shared queues .So the power and area consumption was reduced. A parallel cross bar architecture is proposed in this project in order to reduce the power consumption. Also a new adaptive WXY routing algorithm for multiport router architecture is proposed in order to increase throughput of the network on chip router. The proposed system is simulated using Modelsim and synthesized using Xilinx Project Navigator.

Key words- Buffer, RoShaQ architecture, shared queue, VC router, weighted routing algorithm.

I. INTRODUCTION

Systems on chip design speeding up the system performance through increased the parallelism. Networks on chip are easy to scale for supporting a large number of processing elements rather than point-to-point interconnects wires. In typical router, each input port has an input buffer for temporarily storing the packets when the output channel was busy. The buffer have a single queue means it is a warmhole (WH) router. Multiple queues are in parallel called virtual channel (VC) router[1]. The VC router reduces the significant portion of router area and power compare to the WH router.

In buffer less routers [2] remove the buffers from the router .Its saves much area. But their performance was poor in order to packet injection rates are high. The router has no buffer so contention occurs it should not retransmit the packets. Distributed shared buffer[3] one buffer was used for the all ports so the area of the network was low. The throughput value was increased 7%. Contention was occurred means all packets are dropped. A circuit- switched router, a wormhole router, a quality-of-service (QoS) [5] supporting virtual channel router and a speculative virtual channel router and accurately evaluate the energy-performance. In dynamic voltage frequency scaling (DVFS) reducing the voltage and frequency values when automatically reduce the power value. No control unit required for during voltage and frequency scaling. The power was reduced to 6.3mW.

Other techniques, a dynamic voltage and frequency scaling and globally asynchronous locally synchronous [7] were reducing the power consumption and energy while having only small effect on network performance. A globally-asynchronous locally synchronous (GALS)-compatible circuit-switched on-chip network was used in many-core platforms mainly digital signal processing and embedded applications which typically have a high degree of task-level parallelism among computational kernels. The power consumption was 632μW.the latency also reduced.

Another approach is by sharing buffer queues that utilizing the ideal buffer[8]. The throughput was high. In proposed work differ from the previous work. The router allowing the input packets at input ports to bypass shared queues, it achieves at low load. In the proposed router architecture using a VC router the packets are transferred at high load.

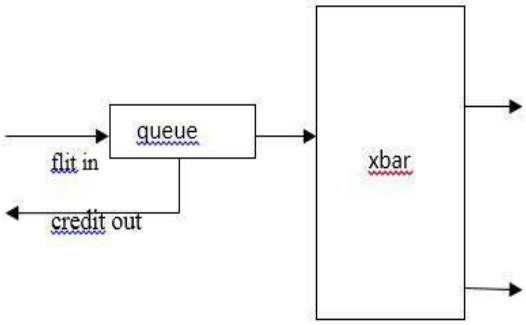
Main contributions of this paper are

1) Analyzing shared queue architectures that maximize the throughput.
2) At high load traffic bypass the input packet to the shared queues in case of reducing the power consumption.
3) Propose shared queue architecture in 8 port router for reducing power and area.

II. RELATED WORK

Warmhole router (WH) single queue was used to store the packets. The flit in was used to send the packet to the queue. The queue was full means the packets were sending

through the credit out. In a WH router, if a packet at the head of a queue is blocked (because it is not granted by the SA or the corresponding input queue of the downstream router is full), all packets behind it also stall. This head of line blocking problem can be solved by a VC router. In this VC router design, an input buffer has multiple queues in parallel; each queue is called a VC that allows packets from different queues to bypass each other to advance to the crossbar stage instead of being blocked by a packet at the head of the queue.



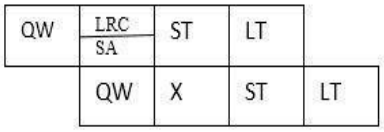
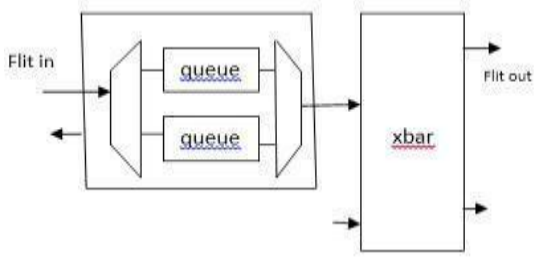


Fig1 WH router



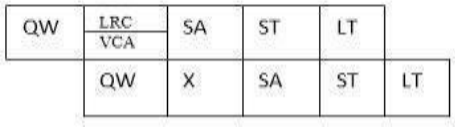


Fig 2 VC router

***A.FIVE STAGES OF VC ROUTER*:**

Step1: At first, when a flit arrives at an input port, it is written to the corresponding buffer queue. This step is called buffer write or queue write (QW).

Step2: Assuming without other packets in the front of the queue, the packet starts deciding the output port for its next router based on the destination information contained in its head flit known as look ahead routing computation (LRC).

Step3: Simultaneously, it arbitrates for its output port at the current router because there may be multiple packets from different input queues having the same output port. This step is called switch allocation (SA).

Step4: If it wins the output SA, it will traverse across the crossbar. This step is called crossbar traversal or switch traversal (ST).

Step5:After that, it then traverses on the output link toward next router. This step is called link traversal (LT).

III. RoShaQ : ROUTER ARCHITECTURE WITH SHARED QUEUES:

RoShaQ, router architecture [6] with shared queues depend on the bypass shared queue architecture. The input queue stores the input packets. The output port stores output packets. The input queues are simultaneously arbitrates both shared queues and output port. When the input queue receives the packet then it calculates its output port to the next router at the time it arbitrates both output port and shared queues. At low load traffic the input packets travel through the input port and shared buffer. More packets send through the router means the time and power consumption was high. Therefore bypass was used to transfer the input packets to output port. Multiple queues are there in the architecture multiple queues are in parallel. The contention occur its send out to the flit out.

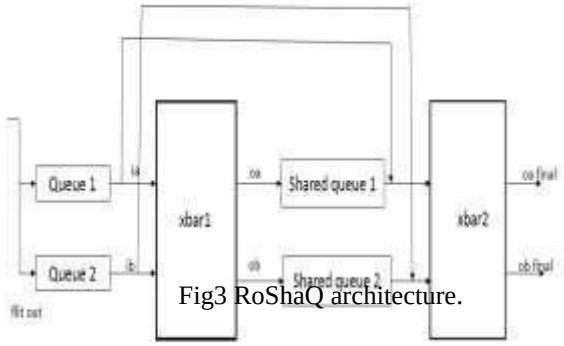


Fig3 RoShaQ architecture.

a) At light load case:

b) high load case:

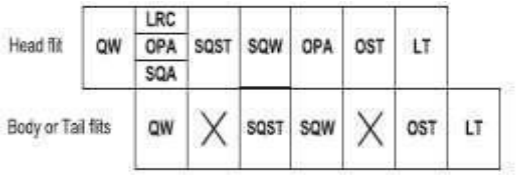


Fig 4 RoshaQ pipeline characteristics (a)four stage at light load.(b)seven stages at heavy load .QW: queue write. LRC: lookahead routing computation. OPA: output port allocation. SQA: shared queueallocation.OST: outputswitch/crossbar traversal. LT: output link traversal. SQST: shared queueswitch/crossbar traversal. SQW: shared-queue write. (X): pipeline bubble or stall.

After a packet is written into an input queue in the first Cycle, in the second cycle it simultaneously performs three operations: LRC, OPA, and SQA. At low load network, there is a high chance to win the OPA due to low congestion at its desired output port; hence it is granted to traverse through the output crossbar and output link toward next router. Therefore, it incurs four stages including link traversal as shown in Fig 4(a) that is similar to a WH router pipeline.

When the load becomes heavy, the packet at an input queue may fail to get granted from OPA, but it can get a grant from SQA and is allowed to traverse the shared-queue Crossbar and write to the granted shared queue in next cycles. After that, it arbitrates for the output port again and would traverse across the output crossbar and output channel toward The next router at next cycles if it is granted by the OPA at this time. Thus, in this situation, it incurs seven inter router stages as shown in Fig. 4(b). This larger number of traversing stages, allows the router to use shared queues for reducing stall times of packets at input queues, hence improves throughput at high load.

In both cases, body and tail flits of a packet traverse through the router in the same way as it head flit, except they do not need to arbitrate for the resources (output ports and shared queues) that are already reserved by the head flit. The tail flit should also release these reserved resources once it leaves the queue.

A.CROSSBAR ARCHITECTURE

The router adds the cross bar control bits to each flit to reduce the congestion level. The crossbar two types of operations are occurred. The crossbar act as a parallel and switch .The operations are depending on the IH (Internal Header).

1) Initialize the input value.
2) Read SELT, WR, CS
3) If SELT=1, WR=0, CS=0 means port
is enable. Else port is disabling.
4) Find the direction of the port
IH=0 means the crossbar works
parallel (e.g.)Output 1= Input 1
IH=1 means the crossbar works like a switch.
(e.g.) Output 1=input 2
5) End the process.

B. RoShaQ's Properties

1) A network of RoShaQ routers is deadlock-free: At light load, packets normally bypass shared queues, so RoShaQ acts as a WH router hence the network is deadlock-free. At heavy load, if a packet cannot win the output port, it is allowed to write only to a sharedqueue which is empty or contains packets having the same output port. Clearly, in this case RoShaQ acts as an output buffered router which is also shown to be deadlock-free.

2) A network of RoShaQ routers is livelock-free: Because both OPA and SQA use round-robin arbiters, each packet always has a chance to advance to the next router closer to its destination; hence the network is also free from live lock.

3) RoShaQ supports any adaptive routing algorithm: The output port for each packet is only computed at its input queue, not at shared queues. Therefore, any adaptive routing algorithm which works for WH routers also works for RoShaQ.

4) RoShaQ can be used for any network topology: If hide all design details inside RoShaQ, we would see RoShaQ only has one buffer queue at each input port similar to a WH router. Therefore, we can change the number of RoShaQ's I/O ports to make it compatible with any network topology known in the literature along with an appropriate routing algorithm.

IV. RESULTS:

Packet 1 and packet 2 are sending through the queue. It was a light load so the bypassing was not used. the packet was send through the input queue and crossbar1 then it will send to the shared queue and send to the crossbar2 finally its stored to the output queue it shown in figure 5.

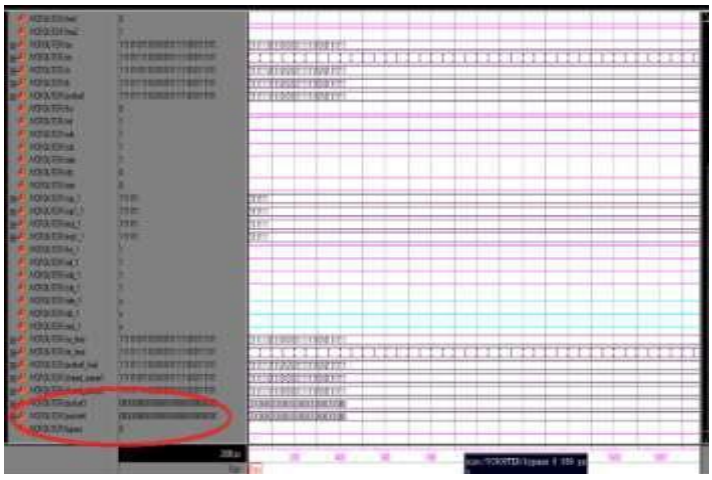


Fig 5 Simulation results at low load traffic.

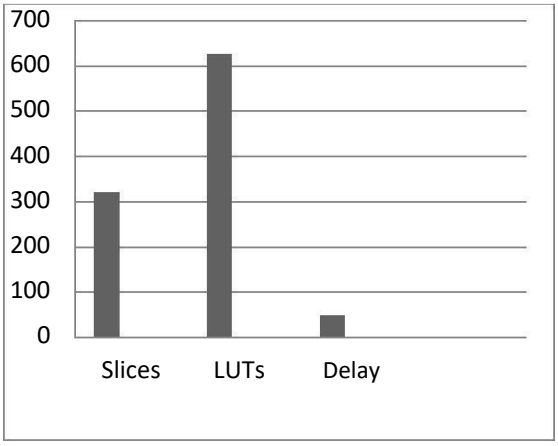
High load are send to the queue means the time consumption was increased therefore the bypasses the input packets to the output queue. The bypass process shown in figure 6.

Fig 6 Simulation results at high load traffic.

V PERFORMANCE ANALYSIS:

The performance of our proposed scheme with existing scheme is analyzed based on the time consumption which was given in table.

Table 1 parameter analysis



VI. CONCLUSION

The shared buffer in virtual channel router is designed and its various stages of packet transmission through the parallel cross bar architecture to reuse the power consumption. Then RoShaQ, router architecture was designed using Type 3 shared buffer architecture.RoShaQ, a novel router architecture thatallowed sharing multiple buffer queues for improving network throughput. Input packets also can bypass the shared queues to achieve low latency in the case

that the network load was low. Compared with a typical VC router, while having thesame buffer space, over synthetic traffic patterns its delay was reduced to 49.95ns.In other methods like VC4 and VC4-fullXbar latency was 33.58 per cycles. In this proposed method the latency was reduced to23.2ns.Lower energy dissipated per packet than typical VC and full-crossbar VC routers, respectively.The gate counts are reduced to 4464, the slices of the router were 322 and the LUTs are 627.

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