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Design and Analysis of Low Power DRAM Cells using Sleep, Stack and Sleepy Stack Techniques

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***Abstract*---Dynamic Random Access Memory (DRAM) is the most common kind of Random-Access memory for personal computers and workstations. Modern advanced processors use DRAM cells for chip and program memory.DRAM stores each bit in a storage cell consisting of a capacitor and a transistor. The advantage of DRAM is its structural simplicity. Due to the nature of its memory cells, DRAM consumes relatively significant amount of leakage power. In this paper, basic DRAM cells are designed using low power design techniques namely, sleep, stack and sleepy stack for leakage power reduction. These DRAM cells are simulated using TANNER EDA tool and comparison ofpower consumption is done for conventional DRAM cells and the proposed cells. It is observed that, among the proposed DRAM cells, cells which employ sleepy stack technique consume less power.**

Index Terms -1T1C, 3T1C, 4T DRAM cell, Leakage power, Sleep, Stack, Sleepy Stack.

I.INTRODUCTION

Memory plays an essential role in electronics design where storage of data is required [11]. The amount of memory required depends on the type of application. On-chip memory has been widely used in Very Large Scale Integration (VLSI) circuits [8]. Semiconductor memory is classified according to the type of data storage and data access. RAM (Random access memory) has become a generic term for any semiconductor memory that can be written to, as well as read from, in contrast to ROM, which can only be read [2].RAM storage is volatile which means that the information can be accessed only when the power is ON [10].RAM is again classified into two types: SRAM (Static Random Access Memory) and DRAM.

SRAM requires at least four to six transistors to store each bit of memory [6]. DRAM requires the data to be refreshed periodically in order to retain the data. DRAM can hold more data than SRAM of same size of chip. DRAM requires only one capacitor tostore each bit of data, butthecharge of the capacitor decreases with time. The advantage of the DRAM is structural simplicity [3] and it is used in high densities. DRAM is used in main memories in personal computers and in mainframes [7].

Leakage current is a major cause of power consumption in a DRAM [4]. The leakage paths in a DRAM cell stem from leakage from the storage node. This leakage contributes to leakage power which can be reduced, by applying techniques like Sleep, Stack and Sleepy stack.

In this paper, we have taken three different DRAM cells such as 1T1C, 4T and 3T1C. Sleep, Stack and Sleepy stack methods are applied for these cells and the power consumption for conventional cells and the modified cells are compared.

II. DRAM CELL TYPES

A.1T1C DRAM Cell

The circuit consisting of one transistor and one capacitor forms the cell structure for 1T1C DRAM.

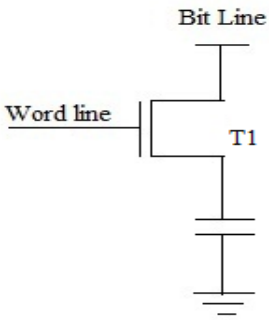

Figure1. 1T1C DRAM Cell

In Figure.1, when the access transistor is turned on by applying a voltage on the gate terminal, a voltage representing the data value is placed onto the bit line and charges the storage capacitor [1]. The storage capacitor then retains stored charge after the access transistor is turned off and the voltage on the Word line is removed. However the electrical charge stored in the capacitor will gradually leak away with the passage of time. To ensure data integrity, the stored data value in the DRAM cell must be periodically read out and written back by the DRAM device in a process known as refresh.

B.Three-transistor DRAM Cell

The information in 3T DRAM cell is stored as in the parasitic capacitor [7]. Figure. 2 shows the structure of 3T cell .Transistors T1 and T3 act as access transistors during write operation and read operation respectively. Transistor T2 is the storage transistor and is turned on or off, according to the amount of charge stored in capacitor. When write signal is enabled, the data is fed into the T1 transistor. When data is to be read from the cell, read line is enabled and data is read through the bit line. 3T DRAM cell occupies less area when compared to the 4T DRAM cell.

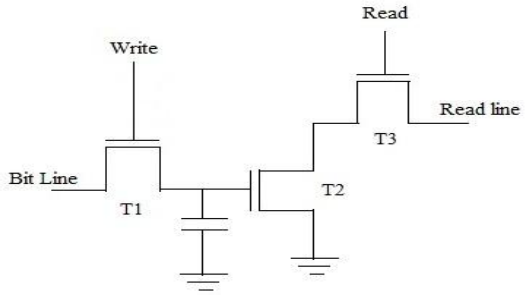

Figure2. Three-transistor DRAM Cell

C. Four transistor DRAM cell

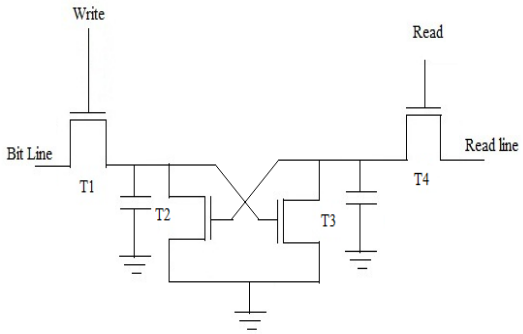

Figure3. Four Transistor DRAM Cell

In 4T DRAM cell, one transistor acts as write transistor and the other as read transistor. In write operation, the word line is enabled and data is stored in the form of charge. There is no current path provided to the storage node, hence data is lost due to leakage, so the data needs to be refreshed periodically. The read operation is non-destructive.

III. Low Power Design Methods

A. Sleep Technique for 1T1C, 3T1C and 4T DRAM Cells

Sleep technique reduces the sub threshold leakage by isolating the gates from power supply and ground. This technique uses the sleep transistor between both VDD and the pull up network and between GND and pull down network [9]. The sleep transistor turns off the circuit by cutting off the power rails in idle mode thus, it can reduce leakage power effectively. This sleep technique is applied for 1T1C, 3T1C and 4T cells.

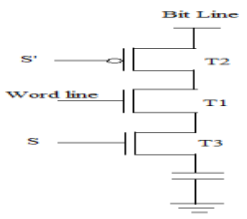

Figure 4. Sleep technique for 1T1C DRAM

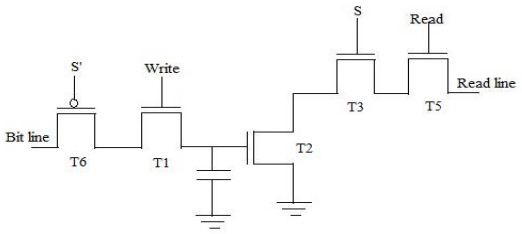

Figure 5. Sleep technique for 3T1C DRAM

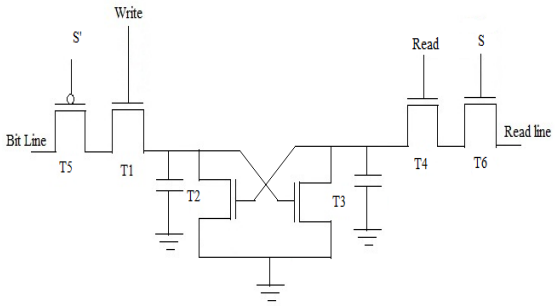

Figure 6. Sleep technique for 4T DRAM

Figure.4 shows the sleep technique applied for 1T1C cell. Here the sleep transistors T2 and T3 are added in addition to T1. Figure.5 shows the sleep technique applied for 3T1C cell. Sleep transistors are T5 and T6. The combination of T1, T2 and T3 represents the conventional 3T1C cell [15]. Figure.6 shows the sleep technique applied for 4T cell. Sleep transistors are T5 and T6. The combination of T1, T2, T3, T4 and capacitors represent the conventional 4T DRAM cell [3].

B. Stack Technique for 1T1C, 3T1C and 4T DRAM Cells

In this approach, the circuit is divided and stacked into two half width of the total transistor size. When these are stacked together, they simultaneously turn on and off. Thus, this technique reduces the sub- threshold leakage current [5]. The leakage through two series OFF transistor is much lower than that of single transistor because of stack effect. But the overall delay of the circuit increases as the number of transistors increases. The dividing of the transistor will not affect the W/L ratio of the circuit. The W/L ratio of the circuit is maintained after dividing the circuit. This stack technique is applied for 1T1C, 3T1C and 4T cells.

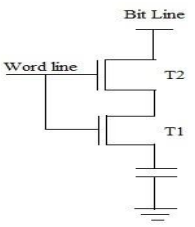

Figure 7. Stack technique for 1T1C DRAM

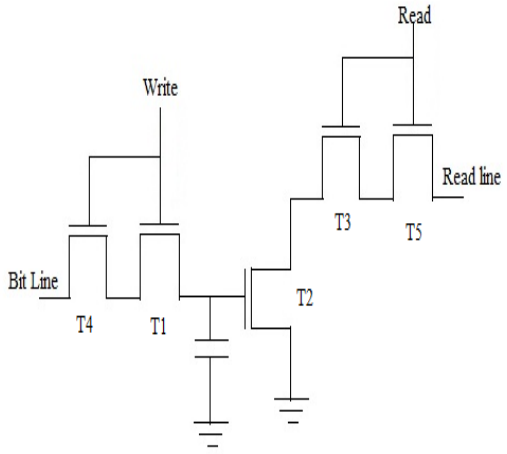

Figure 8. Stack technique for 3T1C DRAM

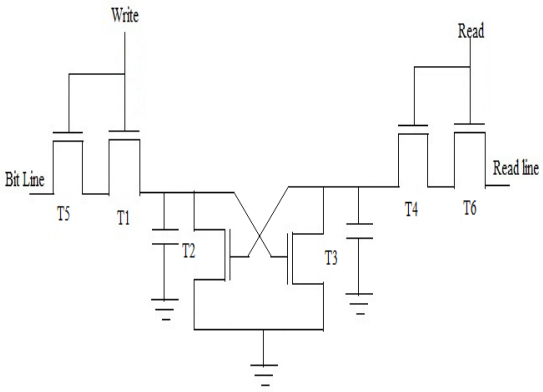

Figure 9. Stack technique for 4T DRAM

Figure.7 shows the stack technique applied for 1T1C cell [12]. Here the original transistor is stacked into two half size transistors T1 and T2. Figure.8 shows the stack technique applied for 3T1C cell. Here the original transistor T1 is stacked into T1 and T4 and the transistor T3 is stacked into T3 and T5. Figure.9 shows stack technique applied for 4T cell. Here transistor T1 is stacked into T1 and T5 and transistor T4 is stacked into T4 and T6. The remaining transistors and capacitors act as storage nodes.

C. Sleepy Stack Technique for 1T1C, 3T1C and 4T DRAM Cells

Sleepy stack technique combines sleep transistors and stack technique. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to the divided transistors [14]. The sleep transistors actions are same as in sleep transistor technique. Since sleep transistors are always on in active mode there is current flow in the circuit and hence has faster switching time than stack approach. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current. The drawback of this technique is increase in area. Here high Vth transistors are used as sleep transistors.

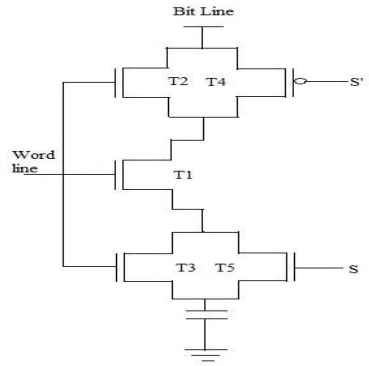

Figure 10. Sleep Stack technique for 1T1C DRAM

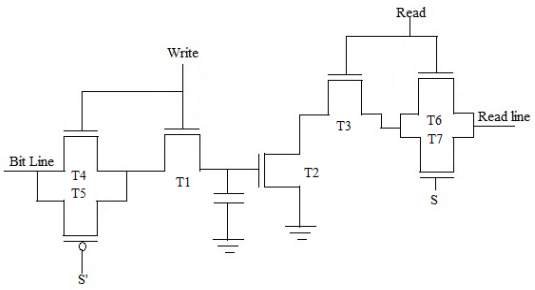

Figure 11. Sleep Stack technique for 3T1C DRAM

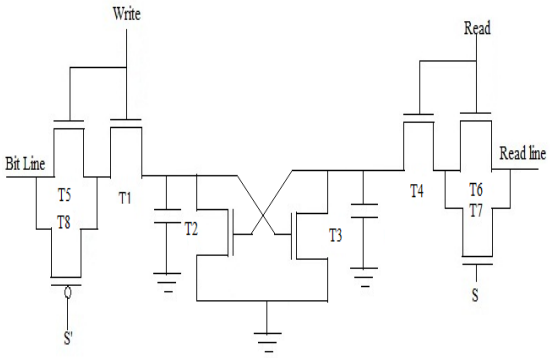

Figure 12. Sleep Stack technique for 4T DRAM

Figure.10 shows the sleepy stack technique applied for 1T1C cell. Here the original transistor is stacked into T3 and T4. Sleep transistors T4 and T5 are added in parallel to T2 and T3 respectively. Figure.11 shows sleepy stack technique applied for 3T1C cell. The original transistor T1 is stacked into T1 and T4 and the transistor T3 stacked into T3 and T6. Sleep transistors T5 and T7 are added in parallel to the stacked transistors. Figure.12 shows sleepy stack technique applied for 4T cell. Sleep transistors are added in parallel to the stacked transistors to get sleepy stack structure.

IV.Simulation Results and Analysis

Sleepy stack technique consumes less leakage power when compared to sleep and stack techniques [2].

Table 1. Comparison of power consumption for 3T DRAM cell

3T DRAM CELL	Power Consumption in Microwatts				
	3V	3.5V	4V	4.5V	5V
Conventional	0.92	1.21	1.57	1.78	1.95
Proposed	0.78	0.79	0.82	0.83	0.85

Table 1 shows the power comparison results of conventional and proposed sleepy stack 3T DRAM cell. It is clear that, powerconsumption for proposed 3T cell is lesser than that for conventional cell for different voltage ranges.

Table 2. Comparison of power consumption for 4T DRAM cell

Table 2 shows the power comparison results of conventional and proposed sleepy stack 4T DRAM cell. It is clear that, power for proposed 4T cell is lesser than that for conventional cell for different voltage ranges.

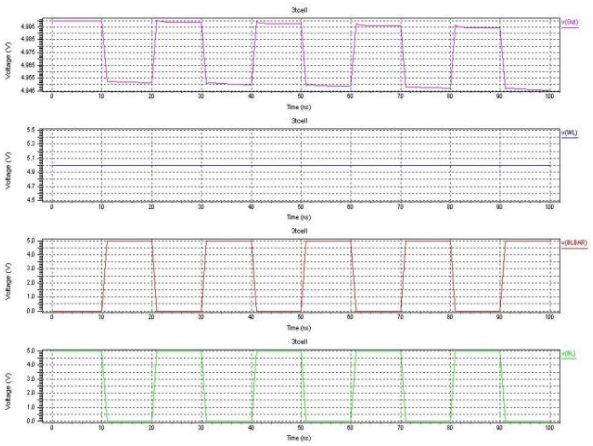

Figure13. Waveform of 3T DRAM cell

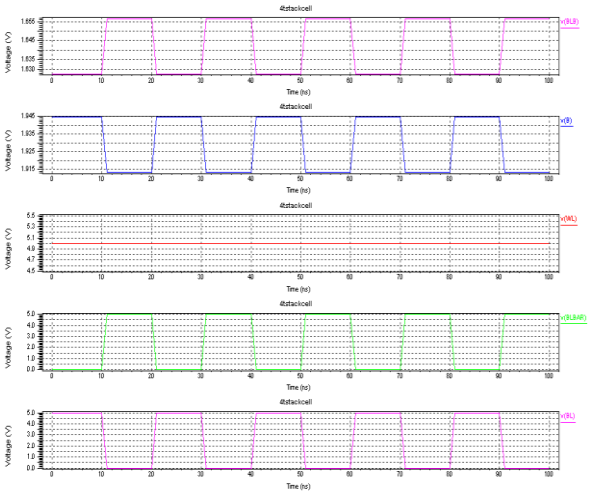

Figure 14. Waveform of 4T DRAM Cell

V. CONCLUSION

In this paper, leakage power reduction techniques are discussed and they are applied to basic DRAM cells. The proposed cells are simulated using TANNER EDA tool and an analysis of power consumption of these cells for different voltage levels is done. Power consumption for the proposed work is less than that for conventional. It is observed that, among the proposed DRAM cells, cells which employ sleepy stack technique consume less power. In future, the proposed work can be applied to memory array structures.

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4T DRAM CELL	Power Consumption in Microwatts				
	3V	3.5V	4V	4.5V	5V
Conventional	1.40	1.85	2.39	3.02	3.03
Proposed	0.92	1.22	1.57	1.78	1.95

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