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Design Of A New Comparator Using A Min Algorithm Operating In Low Power

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Abstract --A comparator in a low-power 180-nm complementary metal–oxide–semiconductor process using a Cadence Virtuoso tool is presented to operate in the low power with the minimum consumption of the power and with the high throughput with high stable nature. Byutilizing the MIN algorithm this could be achieved. The circuit of a conventional type comparator consisting of two cross-coupled inverters is modified for fast operation even with different GHz at low supply voltages. The advantages of a high-impedance input rail-to-rail output swing robustness against the influence of mismatch in the circuit are considered a important and the architecture is designed in a way that to be operate at the maximum frequency along with the minimum power supply.

Index Terms—Comparator, complementary metal–oxide–semiconductor (CMOS) analog circuits, low supply voltage, modified latch, ultradeepsubmicrometer CMOS.

INTRODUCTION

In recent years, exploiting near-threshold and subthresholdcircuits has become a major trend in low-power applications,whichputs forward more critical requirements forlow-output-voltage, small-area, and high-efficiency voltageconverters. In modern system on chips (SoCs), multiple power domains are required for various circuit blocks. Fig. 1 shows anexample of an energy-efficient SoC that utilizes energy-efficient near-threshold logic circuits. Targeting low-power applications, theSoC system uses a power supply for the overall system. The 1-V power supply is directly supplied to analog/RF [5] and I/O [8] circuits. In order to utilize near-threshold operation, a voltageconverter is required to generate a 0.5-V power supply from the1-V input for the logic circuits, with 50-μA to 10-mA outputcurrent range and high power efficiency. Compared with buck/boost dc–dc converters that use inductors, switched-capacitor voltage converter is a preferablesolution for low-voltage power supplies because of great potentialto be fully integrated on-chip. The design challenges of the SC voltage converter are: 1) the degrade efficiency atlow output current I_{OUT}; and 2) the implementation of 0.5-Vvoltage reference circuit and the power penalty dueto V_{REF}. In addition, the design of sub-1V is difficult because a typical operates above 1V. In order tosolve the problems, a low-voltage high-efficiency SC voltageconverter with voltage-reference-free pulse-density modulation is proposed for high power efficiency at low $I_{OUT}$by both reducing the pulse density and eliminating V_{REF} [1].

RELATED WORK

Two major types of conventional comparatorshown in Fig.1. The first type in Fig. 1 usesconstant pulse density for the switch matrix [2]–[4]. Inthis scheme, a non-overlap clock generator is employed to drivethe switch matrix with a fixed clock frequency, as shown inFig. 2. Therefore, it suffers from severe efficiency drop whenoutput current decreases due to excessive clock pulses for smallcurrent demand. Theothertype of conventionalSC voltage converter is attached with the conventional system, which relies on V_{REF} and a comparatorfor pulse-density modulation (PDM) [5]–[9]. The comparatorcompares the output voltage with the reference voltage to performPDM. Therefore, the pulse density is adjusted accordingto different I_{OUT}, thus preventing the efficiency drop due toexcessive clock pulses, as shown in Fig.6. TheV_{REF} is often omitted in the previous works by simply using anoff-chip voltage supply.

This way, the power loss introduced bythe V_{REF} is overlooked. Moreover, a sub-1-V voltage referencemay bring extra design complexity to the voltage converter. Therefore, this scheme costs extra power and area, and it makesthe circuit design complicated with low power supply voltagedue to the use of an on-chip voltage reference. Fig. 3 show the proposed voltage converter andtiming. The key concept of V_{RF}-PDM is to replace the reference voltage in Fig. 2 with the past output voltageV_{OUT}, thereby eliminating V_{REF}. The proposed scheme usestwo sampling clocks, to sample outputvoltage at different times. V_{OUT} is sampled as V_{NOW} andV_{PAST} at each falling edge, respectively. Then, sampled voltages V_{NOW} and V_{PAST} are compared bya comparator with an offset voltage of ΔV. When $V_{PAST} - V_{NOW}$ is larger than ΔV, the comparator output is set to high, and then an expanded pulse signal is generatedas SC_{enable}. Applying an AND gate to CK and SC_enable,a pulse signal SC_clock is to be generated and then fed tothe non -overlap clock generator to drive the switch matrix. Form the existing this circuit is modified by

adding of the keeper circuit with the 0.07%. 0.07% denotes the usage of the keeper for the voltage references, Read path of the circuit is modified with dynamic multiplexer circuit. Circuitis designed with the low power operating condition with help of above mentioned paper. Reponses graphs are created for testing of the circuit.Fig.1.shows the Schematic diagram of the conventional comparator, where the circuit operates without the static power.

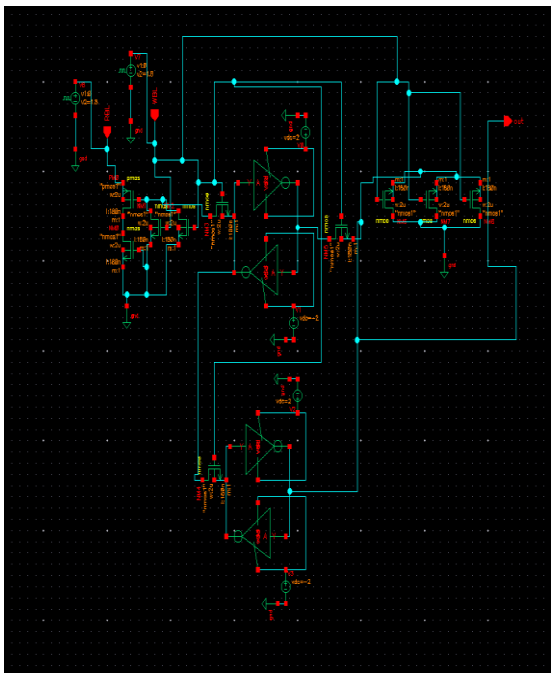

Fig.1. Schematic diagram of the conventional comparator

ADAPTIVE FLOATING-GATE COMPARATOR

The simple circuit shown in Fig. 2 is built with the conventional comparator built using CMOS transistors with PMOS and NMOS transistors which is implemented using theVirtuoso tool, comprising pre-amplification and regenerative stages for the comparison as well as control and localstorage for the adaptation. During normal operation,floatinggate transistors and form the input devices of a differential pair and provide local charge storage. Crosscoupled nFET transistors and forms the regenerative elements of the comparator. When the clock signal is high the nFET switch closes and resets the comparators. When low switch is opens and the evaluation phase begins. The “high” bias voltage on transistor during reset determines conductance of the regenerative elements and there by the overall gain and speed of the comparators. With the power-supply V_{dd} set at the nominal operating voltage of 3 V, there is insufficient electric field between the pFET’s drain and source to produce hot electrons in the channels of and devices. We therefore keep the AFGC’s V_{dd} at 2.5 V during both normal operation and adaptation. V strengthens source-to-drain electric fields there by increasing the energy of electrons in the channels.

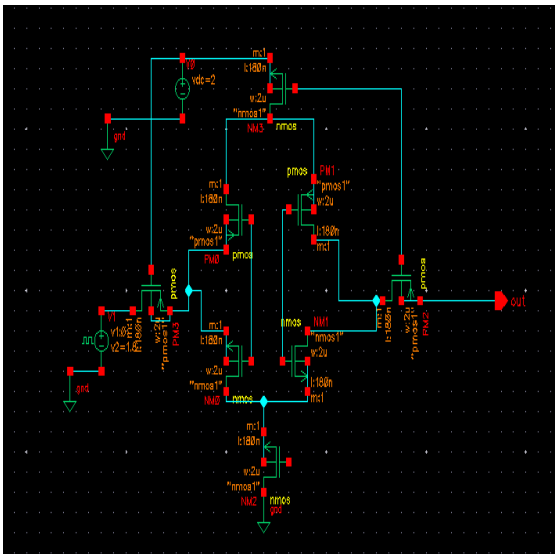

Fig.2. proposed tail comparator for tri state module

Adaptation is controlled by the common-mode input voltage: the common source voltage will follow;so raising enables adaptationby increasing the gatetodrainand sourcetodrain electric fields thus attracting hot electronsonto the floating gate. Conversely lowering disablesadaptation by decreasing the source-to-drain and gatetodrainelectric fields so that fewer hot electrons are generated andso that fewer hot electrons are collected on the floating gate. During adaptation negative charges accumulate on each of thefloating gates, lowering their gate-to-drain and source-to-drainvoltages and establishing negative feedback between the outputsand the inputs to achieve stable adaptation.

While theadaptation mechanism for the AFGC results in reduction inthe common-mode voltage on the floating nodes, all resultsreported in this work include any additional error resultingfrom this shift; thus it does not present a significant limitationto accurate and automatic adaptation. In methods of injection,a static method and a dynamic method. The static method issimple and serves to illustrate the mechanism of calibration, built accuracy is limited in practice. The dynamic injection methodovercomes the accuracy limitations of the simple static methodand provides calibration accuracy under 1 mV; however, duringdynamic injection the adaptation occurs during the evaluationphase so the output of the comparator is latched. This meansthat the update direction cannot change during a single cycle,thus accurate calibration must be achieved over many clockcycles. We also discuss the inherent tradeoffs between speedand accuracy, which can be tuned using the clock voltage. We present Monte Carlo simulations and experimental resultswhich demonstrate the efficacy of calibration using the dynamicinjection method.

ALGORITHM

Step 1: Analyze the circuit for the power conversion for n number of circuit.

$$(\mathrm{Ck})^n = \sum_{i=0}^{n} \binom{nC1}{kCn} xm^k Cka^{n-1}$$

Step 2: Determine the number of conversions to take place and transistors to be used in the conversion process

$$(\mathrm{nKt})^n = 1 + \frac{tnx}{n1!} + \frac{tn(rn-t1)x^2}{n2!} + \cdots$$

Step 3: Register cells in the path along with the voltage converter are taken and external charge storage devices are taken

Step 4: Along with the voltage converter the device for the conversion are attached with the memory cells in the read path

Step 5: to the readpath the voltage converter the frequency range is to be set in the input devices.

Step 6: pulse input is given as input to the device, and DC voltage are taken for the references.

A. Static Injection Method

The static injection method accomplishes adaptation byapplying a constant voltage bias to the clock terminal. When the clock is high, the comparator becomes an amplifierwhose differential inputs and differentialoutputs are related by a finite voltage gain. The constantis the capacitance ratio, where is the capacitancebetween nodes, and is the total capacitance coupled to the floating node. The voltage gain from floating nodes andto the differential outputs is greater than the overall voltagegain. The goal of offset cancellation is to balance thedifferential output when the input difference iszero. Suppose that mismatch causes the outputsto be unbalanced when the inputs are equal. WhenV_{dd} is sufficiently high, injection occurs when thecommon-mode input voltage is raised.Since the source-to-drain voltage of is greater than thatof , the injection current onto the floating gate ofwill be greater than the injection current at and thefloating-gate potential will decrease faster than . Asa result, the differential current will increase with a concomitantdecrease inV_{dd}, causing the output voltage to riseand to fall. This feedback cycle will drive the floating-gatevoltages and to values that compensate for the initialdevice mismatches. The input-referred offset after calibration depends on earlyvoltage, voltage gain and mismatch of both device and injectionparameters.The load operation in the system,

$$\mathrm{Y}\,\alpha + \mathrm{load}\,\beta = 2\,\mathrm{C}\frac{1}{2}(\alpha r + \beta)\,\mathrm{Cx}\frac{1}{2}(\alpha - \beta r)$$

Dynamic Injection on the Floating Gates

We describe a dynamic injection technique which overcomesthe overshoot problem observed when using static injection.The dynamic technique achieves injection during the evaluationphase when the clock signal is low and the comparatoris latched, with adaptation achieved over many evaluation cycles.By injecting with a running clock, we use the outcomeof each comparison to correct offset during the correspondingevaluation cycle. Thus, the feedback loop encompasses all mismatchand offset within the circuit, and accurate offset cancellationcan be achieved. We bias the common-mode input voltageso that the drain-to-channel voltage is insufficient for injectionduring the reset phase of the clock cycle, but sufficientto produce injection during the evaluation phase when one ofthe outputs or is close to ground.

Trade-offs Between Resolution and Speed

Since offset resulting from device mismatch can be cancelled,the resolution of the AFGC is determined by the input-referrednoise. For perfectly calibrated devices, the error introduced bythis noise will be random and may be reduced by examiningthe comparator's outcome over many evaluation cycles. Whenthe devices are not perfectly calibrated, the residual offset contributesan additional source of input-referred noise which is deterministic. Under realistic conditions, this deterministic noiseis smaller than the random noise (see above). The relative magnitudesof the deterministic and random noise sources are determinedby the injection mismatch ratio. The power of the controller is determined by

$$P = V_0 + Ir + m$$

CIRCUIT DESCRIPTION

The circuit of the proposed comparator is shown in Fig. 3. Incontrast to the conventional comparators latch used in Fig. 1, where only N0and N1 are initially on, the latch of the proposed comparatoris expanded into two paths between the supply rails (transistorsN0, N1, P0, P1, P4, and P5), so that, at the beginning of thecomparison phase, where both output nodes have the initial condition OUT = OUT = VCO (initially, internal nodes FB =FB = VSS), transistors N0 and N1 are turned on. However, transistors P0 and P1 are also turned on and build, with inputtransistors N2 and N3, an amplifier with a distinct workingpoint, which, in contrast to that in Fig. 3,which shows the overall schematic of the module, contributes enoughgate–source voltage to transistors N0 and N1 at lower supplyvoltages. Complete positive feedback of the latch starts whenone output node is discharged enough to turn on P4 or P5.

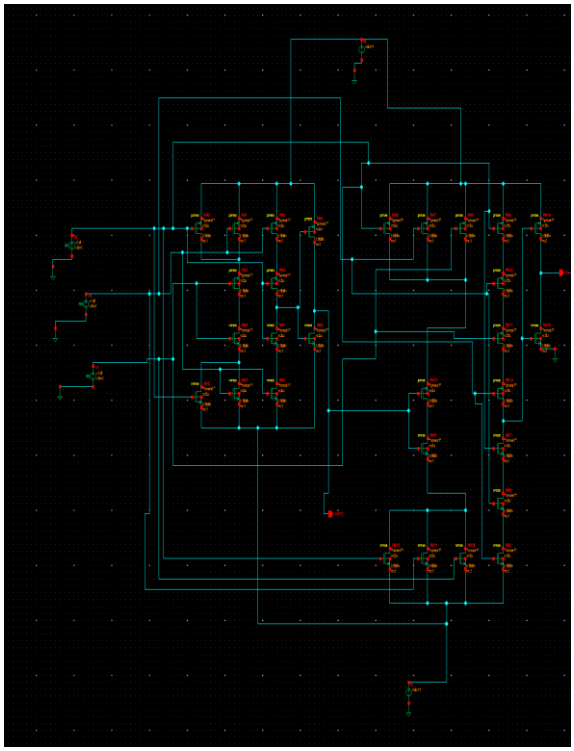

Fig.3. Proposed schematic of the comparator

Regeneration is done with N0, N1, P0, and P1, where P4 and P5help with additional amplification. To get a rail-to-rail outputswing and no static power consumption of the comparator,one of the initial load transistors P0 or P1 is switched off, when, during regeneration, FB or FB, respectively, is chargedto VCo. The other advantages of a high-impedance input and nodirect influence of parasitic capacitances of N2 and N3 to theoutput nodes are kept. The corresponding transient simulationsof Fig. 6 can be seen in Fig. 7. A clock period is divided into twophases: The reset phase (CLK = VSS) is used to establish theinitial condition OUT = OUT = VCo for the following comparisonphase. (CLK = VCo, VCo is the positive supply voltageof the comparator.) During reset, transistor N6 is switched off, and transistors P2, P3, N4, and N5 are on.

A carrier is described by

$V = V_c \sin(\omega_c t + \theta)$

$v = \{V_c + V_m \sin(\omega_m t)\} * \sin(\omega_c t)$

Active Diode

Fig. 4 shows the schematic of ancomparator consisting ofa tristate system with a PMOS. In this specific implementation, thedrain and source terminals are equivalent to the anode and cathodeterminals of a diode. The comparator monitors the voltagebetween the two terminals. When the anode voltage is higherthan the cathode, the comparator outputs a low voltage to thegate terminal to turn ON the PMOS. Otherwise, a high outputwill be generated to turn OFF the PMOS. In this manner, theactive diode behaves as an ideal diode. The conduction voltagedrop of the PMOS is much smaller than the forward-bias voltagedrop of a junction diode, and the on-resistance is usuallysmaller, too. Also, the leakage current in the OFF state can bemuch smaller than reverse leakage of a junction diode. Despite these advantages, there are several drawbacks withan active diode. First, external supply voltage and power isrequired for the comparator. In an energy harvesting system, this requires a continuous supply of energy from thesource or load, as well as a mechanism for self-starting (bootstrapping)from a completely discharged state. Fortunately, thepower consumption is quite low; comparators with <1 μWstatic power consumption are readily available from commercialvendors, and even lower power comparators may be designedby eliminating unnecessary functions found on commercial ICs.These issues are further discussed in the following. Anotherdrawback of the active diode is that the ON and OFF stateof the PMOS is controlled by the differential voltage betweenits gate and source. Since the source terminal is on the signalpath with volatile potential, a floating control is required, whichrequires careful design because the control voltage (VGS) is alsoinfluenced by the input signal.

Voltage Doubler Using Active Diodes

The active diode is configured as a voltage doubler. The circuit consists of a positive and a negative peakdetector, generating dc voltages that track the positive and negativepeaks of the input. Therefore, a dc voltage of twice the input amplitude can be obtained. When active diodes are used,the conduction voltage drop is much smaller than junction diode,and the circuit can operate at very low input voltage amplitude. While the power requirements for the active diode are expectedto be small, the source of the external power must stillbe considered. A complete energy harvesting system can beexpected to have an energy storage unit (e.g., rechargeable battery),as shown in Fig. 3. Here, the battery load provides voltagesupply to the comparators in the voltage doubler to enable ac/dcrectification. The input ac voltage is rectified to a dc voltage thatis twice the ac amplitude. The low dc voltage is then boostedby a boost converter to a voltage level sufficient to charge thebattery. As long as the charging current is higher than the supplycurrent of the comparators, the battery can be charged. In practice,a limit on the battery discharge could be set, so that therewould always be sufficient charge and voltage for the activediode operation.This system configuration is plausible by using commerciallyavailable ultralow-power comparators and low-voltageboost converters. For example, the comparator used in this paper can work with supply voltage/current of 2.5 V/560 nA [13]. An ultralow-voltage boostconverter LTC3108 from Linear Technology can provide an outputvoltage of 2.35 to 5 V with only 20 mV of input voltage [14].Additionally,

several other academic efforts have aimed to reducethe input voltage and increase the efficiency of boost convertersfor energy harvesting applications [15], [16].Note that in this design, the source terminals of bothMOSFETs are connected to the capacitors. Such arrangementhelps to reduce the volatility of the source potential. Also, ifthe comparator power supply terminals are connected to thepositive/negative output terminals of the voltage doubler, andthe input voltage is high enough, the comparators may functionwithout an external power supply. Under these conditions,the power feedback mechanism shown in Fig. 2 could be eliminated. This input-powered functionality is verified in Section III-D.

For complex Z=X+i*Y, EXP(Z) = EXP(X)*(COS(Y)+i*SIN(Y)).

```
x = [0:pi/36:2*pi];
y = cos(x);
plot(x*180/pi,y)
xlabel('x(degree)'), ylabel('cos(x)')
```

Circuit Dynamics

The dynamics of the circuits are analyzed to help select componentparameters, so that proper functionality and high efficiencycan be achieved. As the basic building block of the voltagedoubler, the active-diode-based peak detector is analysed to provide insight into the whole circuit. The steady-state opencircuitvoltage of the peak detector is calculated with comparatorhysteresis taken into consideration.

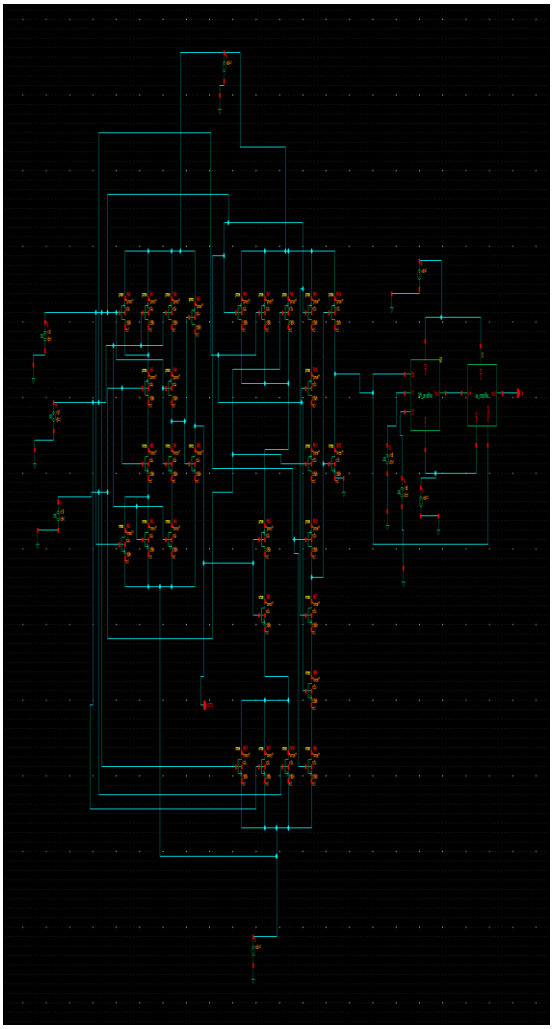

Fig.4. overall proposed comparator circuit

Comparator Hysteresis:

An ideal comparator has perfectzero-crossing detection function; however, typical comparatorshave hysteresis that creates some small error. Some comparatorseven intentionally add hysteresis to reduce sensitivity to noise.For active-diode application, since the differential input voltageof the comparator is the product of the drain to source currentand on-resistance of the MOSFET, the voltage is usually verysmall. In order to detect the small input signal, the comparatorhysteresis should not be too large. In Cheng et al.'s previouswork [12], comparators with a hysteresis band of ±2 mV wereused, and the output did not reach steady state until a stabilizationnetwork was added. To understand the effect of hysteresis,two cases (MOSFET turning ON and MOSFET turning OFF)are considered in the following. First, when theMOSFETis initially turned OFF, the comparatorshould be able to turn ON the MOSFET when the sourcevoltage is higher than the voltage on the capacitor. Ideally, theMOSFET will turn ON as long as the source voltage is higherthan the capacitor voltage by an infinitesimal amount, so thatthe capacitor voltage should precisely track the peak. However, the differential voltage has to exceed the comparator hysteresisvoltage in order to turn ON the

MOSFET. This is illustrated inFig. 4. In the extreme case, if the initial capacitor voltage istoo close to the maximum voltage of the source, the MOSFETwill never turn ON, and the peak will be missed, as shown inFig. 4.Second, if the MOSFET is initially ON, it needs to be turnedOFF whenever the source voltage is lower than the voltage onthe capacitor (or current reflow is detected).

y=-2.5*a:.05*a:2.5*a;
XMA2 = (X-a).^2; XPA2 = (X+a).^2; Y2 = Y.^2;
FCXY = c*((Y./(XMA2+Y2))-(Y./(XPA2+Y2)));

However, becausethe minimum detectable voltage exists, the MOSFET will notturn OFF until the capacitor voltage is already higher than thesource voltage by a finite value. This is illustrated in Fig. 5. Asan extreme case, if the maximum voltage difference between thecapacitor and the source is smaller than the minimum detectablevoltage, the MOSFET will never turn OFF, and the capacitorvoltage will just follow the source, as shown in Fig. 5.It seems obvious that a comparator with no hysteresis willprovide optimum solution. In reality, however, a certain degreeof noise rejection is sometimes desirable, since the comparator output oscillation due to noise will increase the power consumption.Therefore, a small hysteresis voltage may be desirable, aslong as the stability of the circuit can be maintained. This isfurther studied in the next section.

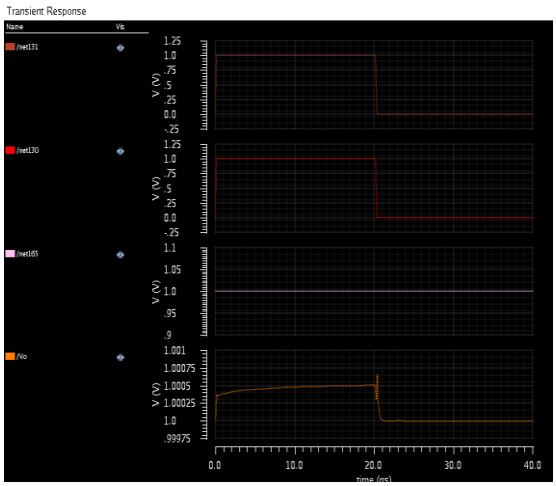

Fig.5. Transient analysis

Active-Diode-Based Peak Detector Open-Circuit Steady-State Capacitor Voltage Analysis:

In order to determine hysteresis voltage can be tolerated; an analytical solution ofthe open-circuit steady-state waveform is derived for an activediode-based peak detector (one half of the voltage doubler circuit).The circuit variables are labelled in Fig.6, and the analysisis based on the following assumptions. The source waveform is given by vin (t) = Vin sin(ωt),and the static voltage on the capacitor is V_{c0} before theMOSFET is ON. The voltage doubler was built and tested using discrete componentsto demonstrate and characterize the design concept.

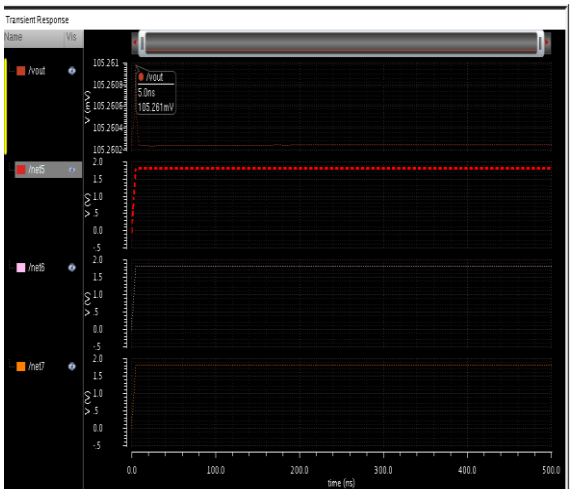

Fig.6. Transient analysis -2

Transient analysis are analysed with the proposed comparator. Different voltages are applied over the proposed converter, for the 0.8V input voltage 204.65mV is produced as an output with the reduced low voltages under the high throughput with the less power consumption to the devices. Two different transient analysis are used for the physical comparisons states between the two proposed tri state comparators.

Open-Circuit Measurements

Before applying a load, the open-circuit waveform was firstmeasured under different amplitudes and frequencies. With20 Hz sinusoidal input, the circuit exhibited minimum inputvoltage amplitude of 5 mV. This lowerbound was the point, where the output voltage and input amplitudediffered by ~10%. A frequency swept was also performedwith 0.25 V amplitude sinusoidal input from 1 to 500 Hz. Asthe frequency increased, the output waveform started to be distorted.

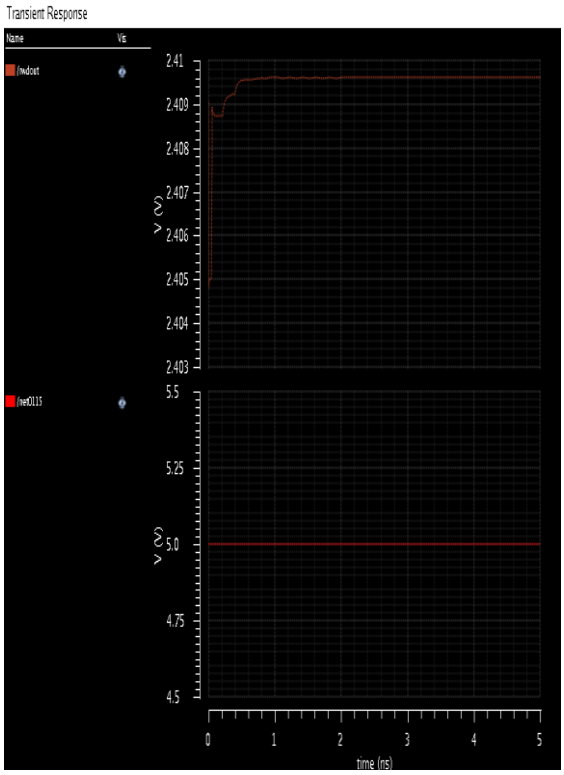

Fig.7. Transient analysis -3

Efficiency and Power Measurements

Using a pulse input waveform, the measured efficiencyfor different input amplitudes and different load resistancesis plotted. The power efficiency is calculatedbyEfficiency =Load powerInput power + External power× 100%. (12)Greater than 80% efficiency was achieved for input voltage amplitudeshigher than 0.25Vfor load resistances from 100Ωup to5 kΩ. Also note that the efficiency was not sensitive to the inputvoltage amplitude for voltages between 0.25 to 1.2 V (∼10%variation). A possible explanation is as follows. When the inputvoltage increases, two things happen.

TABLE I:

	Proposed Dynamic Comparator	**Dynamic Comparator [1]**
Technology CMOS	180 nm	180 nm
Supply voltage (V)	0.8	0.8
Maximum sampling frequency	3.4 GHz	2.4 GHz
Delay	246	294
Energy per conversion	0.20p	0.24p
Estimated area	22 μ ×10 μ	28 μ ×14 μ

First, the voltage magnitudeon the capacitors (MOSFET source terminals) increase, and the gate to source voltage of theMOSFETs decrease, resultingin increased on-resistance of MOSFETs and decreased loadpower/input power ratio. Second, the absolute input power is increased and the fixed comparator power consumption becomesless important, which tends to increase the overall efficiency. The combined result of these two contradicting effects makesthe overall efficiency less sensitive to input voltage. Under the same testing conditions, the output power is plottedin Fig. 7. The extracted output power ranged from microwattsto tens of milliwatts, scaling approximately proportional to theinput voltage squared. The maximum power was consistentlyachieved at 100 Ω, regardless of the input voltage. This is closeto the output impedance of the circuit when both MOSFETare OFF (∼130 Ω). This makes it more convenient to performimpedance matching at the next stage.

CONCLUSION

In this work, a comprehensive delay analysis for clocked dynamic comparators along with the new comparator design for functioning with the processor is designed. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators with the special multi comparator are designed with the reduced area were analyzed. Also, based on analyses a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 180nm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and multi-tail comparator.

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