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Design Of 2/3 Prescaler Using Pass Transister Logic For Frequency Divider

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***Abstract*- An extended true-single-phase-clock (E-TSPC) based divide-by-2/3 counter design for low supply voltage and low power consumption applications is presented. By using a wired OR scheme; only one transistor is needed to implement both the counting logic and the mode selection control. This can enhance the working frequency of the counter due to a reduced critical path between the E-TSPC flip flops (FFs).Since the number of transistor stacking between the power rails is kept at merely two, the proposed design is sustainable to low operations(531 MHz at 0.6 V) for the power saving purpose. Simulation results show that compared with two classic E-TSPC based designs in 0.18 nm process technology, as much as 16.4% in operation speed and 39% in power-delay-product can be achieved by the proposed design.**

Index Terms-Extended True Single-Phase-Clock flip flops(E-TSPC FF),low power,low voltage,prescaler.

I. INTRODUCTION

High speed divide-by- counter (also called prescaler) is a fundamental module for frequency synthesizers. Its design is crucial because it operates at a higher frequency and consumes higher power consumption. A divide-by- counter consists of flip-flops (FF)and extra logic, which determines the terminal count. Conventional high speed FF based divide-by counter designs use current-mode logic (CML) latches [1] and suffer from the disadvantage of large load capacitance. This not only limits the maximum operating frequency and current-drive capabilities, but also increases the total power consumption. Alternatively, FF based divide-by designs adopt dynamic logic FFs such as true-single-phase clock (TSPC) [2]–[4]. The designs can be further enhanced by using extended true-single-phase-clock (E-TSPC) FFs for high speed and low power applications [5]–[10]. E-TSPC designs remove the transistor stacked structure so that all the transistors are free of the body effect. They are thus more sustainable for high operating frequency operations in the face of low voltage supply. Past optimization efforts on prescaler designs focused on simplifying the logic part to reduce the circuit complexity and the critical path delay. For example, an E-TSPC design embedded with one extra pMOS/nMOS transistor can form an integrated function of FF and AND/OR logic [7]. Moving part of the control logic to the first FF to reduce unnecessary FF toggling yields another version of prescaler design[8]. These two classic designs each contains 16 transistors only and the mode control logic uses as few as 4 transistors. To achieve such circuit simplicity, it calls for a ratioed structure in the FF design. Despite its distinct speed performance, the incurred static and short circuit power consumptions are significant. Latest designs presented in [10] adopt a general TSPC logic family containing both ratioed and ratioless inverter alternatives. Since the maximum height of transistor stacking is up to 5, these designs lose their performance advantages when working under a low scenario. In [11], a power gating technique by inserting an extra pMOS between and the FF is employed in two novel divide-by-2/3 counter designs. The unused FF can be shut down when working in the divide-by-2 mode. Due to the increase in the number of transistor stacking (up to 4), these designs are not suitable for low operations.Due to the quadratic dependence of power consumption on supply voltage, lowering is a very effective measure to reduce the power at the expense of speed performance. In this paper, a prescaler circuit design aimed at tackling the speed and power issues simultaneously using non-state-of-the-art process technology (0.18 m) is presented.In particular,we focus on low operations for power saving without sacrificing the speed performance. In this design, ratioed E-TSPC FFs are employed due to its circuit simplicity and speed performance. Only one pass transistor is needed to implement the mode control logic. The proposed design in capable of working at a maximum frequency of 531 MHz when the supply voltage is as low as 0.6 V.

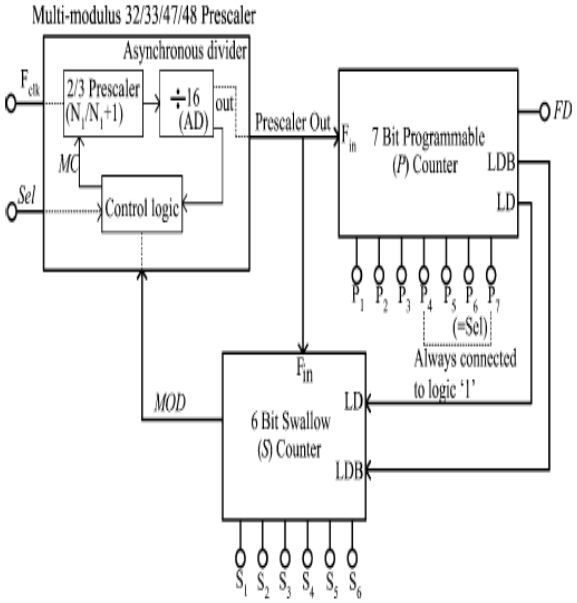

Figure 1. Proposed Dynamic Logic Multiband Frequency Divider

Ii.Design Considerations

The key parameters of high-speed digital circuits are the propagation
delay and power consumption. The maximum operating frequency of a digital circuit is calculated by the method described and is given by

$$f_{max} = \frac{1}{t_{pLH} + t_{pLH}}$$

The total power consumption of the CMOS digital circuits is determined by the short - circuit power. The switching power is liner- ly proportional to the operating frequency a-nd is given by the sum of switching power at each output node as in

$$P_{switc\,hing} = \sum_{i=1}^{n} f_{clk}\, C_{Li} Vdd^2$$

Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{SC} = I_{sc} * V_{dd}$$

The short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem.

The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18-µm CMOS process.

Iii.Proposed Divide-By-2/3Counter Design

The logic structure of the proposed design is shown in Fig. 2. The two FFs and the AND gate are common in previous designs. The OR gate for the divide control is replaced with a switch. Note that there is a negation bubble at one of the AND gate's input. The output of FF1 is thus complemented before being fed to FF2. When the switch is open,the input from FF1 is disconnected and FF2 alone divides the clock frequency by 2.When the switch is close, similar to the design in [7], FF1 and FF2 are linked to form a counter with three distinct states. Fig. 3 shows the circuit implementation. According to the simulation results given in [12], E-TSPC design shows the best speed performance in various counter designs including the one using conventional transmission gate FFs. Besides the speed advantage, E-TSPC FFs are particularly useful for low voltage operations because of the minimum height in transistor stacking. Other than the two E-TSPC FFs, only one pMOS transistor is needed. The pMOS transistor controlled by the divide control signal serves as the switch. The AND gate plus its input inverter are achieved by way of wired-AND logic using no extra transistors at all. The proposed design scheme is far more sophisticated than the measure of simply adding one pass transistor may suggest. First of all, unlike any previous designs, the E-TSPC FF design remains intact without any logic embedding. Both speed and power behaviors are not affected, which indicates a performance edge over the logic embedded FF design. Secondly, the inverter to complement the one of the two E-TSPC FF outputs for divide-by-3 operations is removed in the proposed design. The circuit simplification, again, suggests the improvements in both speed and power performances. The working principle of the proposed design is elaborated as follows. When is "1", the pMOS transistor is turned off as a switch should behave. A single pMOS transistor, however, presents a smaller capacitive load to FF1 than an inverter does in design [7]. When is "0", the output of FF1, , is tied with the output node of the 1st stage inverter of FF2 through the pMOS transistor. In an E-TSPC FF design, the output of the first stage inverter can

be complementary to the input, i.e., . Therefore, a wired-OR logic is in fact implemented.

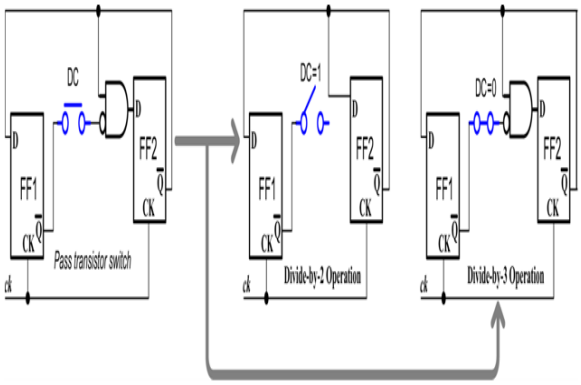

Figure 2. Logic structure of proposed divide-by-2/3 counter design.

Iv.Swallow (S) Counter

The 6-bit s-counter consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The asynchronous bit-cell used in this design shown in Fig. 6 is similar to the bit-cell reported . In the initial state, MOD=0, the multimodulas prescaler selects the divide-by-(N+1) mode (divide-by-33 or divide-by-48) and counters start down counting the input clock cycles. When S counter finishes counting, MOD switches to logic "1" and the prescaler changes to the divide-by-N mode (divide-by-32 or divide-47) for the remaining (P-S) clock cycles.

V.Programmable(P)Counter

The programmable -counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. When the p counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in P counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0"(MOD=0) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved.

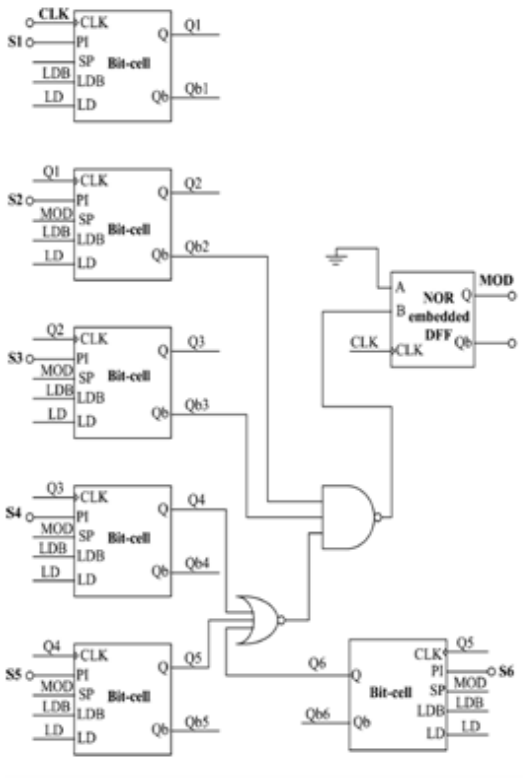

Figure 3. Asynchronous 7-Bit S-Counter

When logic signal sel=0, the prescaler act as 32/33prescaler .The frequency division ratio of multiband divider is given by

$$FD=(N+1)*S+N*(P-S)=NP+S.$$

When logic signal sel=1,the prescaler act as 47/48 prescaler. The frequency division ratio is given by

$$FD=(N*S)+(N+1)*(P-S)=(N+1)P-S$$

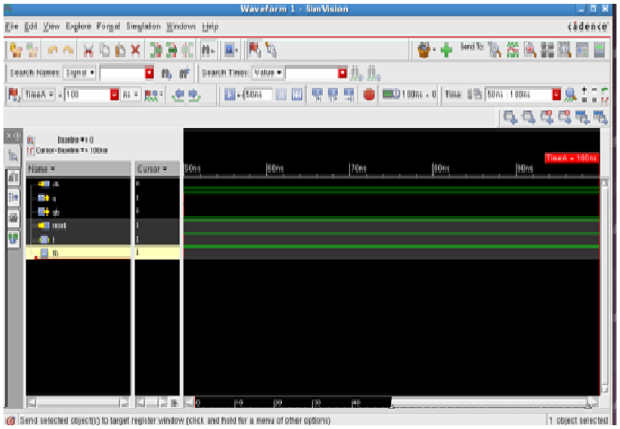

Figure 4. Simulation Waveform Of Swallow Counter

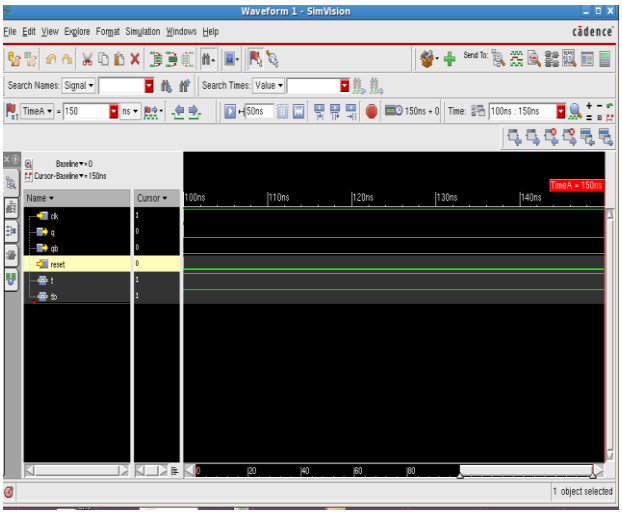

Figure.5. Simulation Waveform of Programmable Counter

VI.CONCLUSION

In this paper demonstrated that pass transistor logic system has considerable implementation.It is proposed for power reduction. The operations of multimodulas prescaler are according to their modes of operation. Here the input frequencies are divided into multiple ranges while the power consumption is reduced. A multimodulas prescaler are verified and multiband flexible divider is verified. In this project provides solution to the low power, PLL synthesizer is implemented. The proposed multiband flexible divider consumes power 52 mw. In future work, we are going to reduce the power consumptions and achieve maximum operating frequency and also reducing the complexity of the circuits using pass transistor logic.

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Authors Profile

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