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Design And Implementation Of Low-Power And High Speed 128-Bit Regular Square Root Carry Select Adder

A.Manikandan[1], R.Lokeshwaran[2], K.Prabhakaran[3], P.Mathialagan[4]

B.E ELECTRONICS AND COMMUNICATION ENGINEERING, SNS COLLEGE OF TECHNOLOGY.

ABSTRACT:

In processors, data processing mainly depends upon speed, area and power consumption. Adder circuit is the main building block in DSP processor. 64 bit CSLA is the fastest adder circuit which was used in processors to perform fast arithmetic operation is a challenging task. This paper proposes a regular 128 bit regular SQRT CSLA which has reduced area, low power consumption, increased processor speed and uses the efficient gate level modification when compared to regular 64bit CSLA. The simulation result shows that regular SQRT CSLA structure is better than conventional CSLA structures. . In mobile and telecommunication the reduction in area and power plays a major role since the portability and the efficiency which increases the performance.

KEYWORD*:* SQRT CSLA (square root carry select look ahead adder), RCA (ripple carry adder), CLA (carry look adder).

INTRODUCTION*:*

In the VLSI the designing of the low area and high performance system is the most important area of research. CSLA is used in many computational systems to avoid the carry propagation delay by generating multiple carries and then select a particular carry to generate the sum. Adders not only used in processor, but also in other Parts of processors where they are used to calculate addresses, table indices. Some other application of adders in MEC (multiply accumulate). The Ripple Carry adder is very compact in design but, it takes a longer time. Adders also used in multipliers, high speed IC's and in Digital Signal Processing to execute FIR, FFT, IIR. The regular 128-bit CSLA will act as a compromise between the area performance and the power consumption. Dual RCA pairs considering the carry input as Cin=0 and Cin=1 then final sum and carry is selected through multiplexers. Linear and square root CSLA are the common types. The Carry Select Adder is used to overcome the propagation delay generated by the Ripple Carry Adder.

SQRT CSLA:

It uses ripple carry adder (RCA). RCA uses less number of logic gates than N-bit full adder. The circuit uses EX-OR gate, OR gate and multiplexers. The multiplexer is used for selecting the correct carry. These components comprises the regular SQRT CSLA. The output carry of previous adder becomes the carry input to next full adder. The output obtained will be selected using

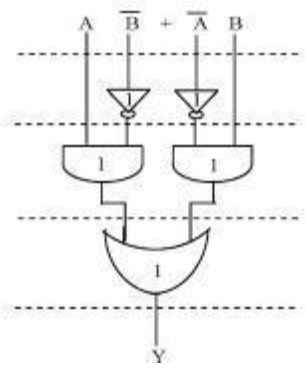
the multiplexers. So that error in the output will be neglected using the multiplexers.

Small area and larger delay will be there in RCA. Large area and small delay will be present in CLA. As the value of N (Number of adders) increases the delay of adder will also increase in a linear way because of large propagation delay. But it occupies least area. SQRT uses many groups of different size RCA and MULTIPLEXER.

Conventional adder has a main disadvantage that uses large area. To overcome this defect this paper is proposed with regular SQRT CSLA. Time delay in conventional adder can be decreased by having one more input into each set of adders than in previous set. Selection input of 8:4 mux is used. If MUX=0 then multiplexer select first RCA output Cin=0 or else second RCA output Cin=1 is selected.

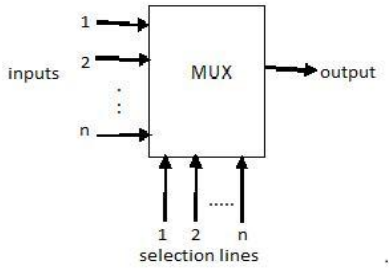
DELAY AND AREA EVALUATION OF BASIC ADDER:

The delay of the basic adder are calculated using the basic gates such as AND, OR and INVERTER (NOT) by implementing XOR gate using above gates. The gates (between the dotted line) performs the parallel operation. By counting the number of AOI the area calculation can be done easily. The delay of this adder is equal to 1 unit and area is also equal to 1 unit.



MULTIPLEXER:

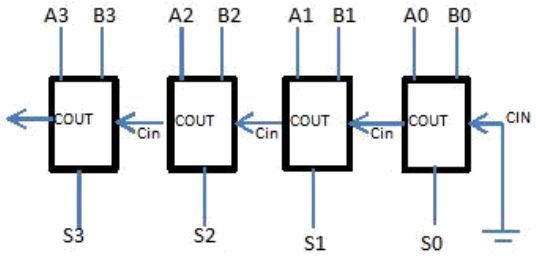
Multiplexer is called as “MUX”. It is a combinational circuit and has several inputs and single output. It has 2^n inputs and n selection lines. It is also called as data selector. It is used in data routing, logic function generation, parallel to serial conversion and etc.



RIPPLE CARRY ADDER:

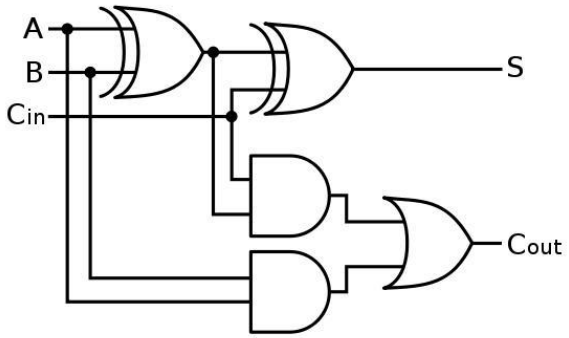
In multiple full adder logic circuits in which carry out of one full adder is given as carry –in to the next full adder which are cascaded in parallel to add N-bit of numbers

.It is called ripple carry adder because each carry bit of one stage is rippled to the another stage. Circuit diagram of 4-bit ripple carry adder is given below to understand better.



FULL ADDER:

To understand the working of ripple carry adder, then you should look at the full adder. It adds three 1-bit numbers, ie). Two input operand bit and one carry in bit (A, B, Cin). It usually component in cascade of adders which adds 16, 32, 64, etc. bit of binary numbers. This circuit produces two outputs, sum and carry represented by 'S' and 'Cout' respectively. The diagram is given below,



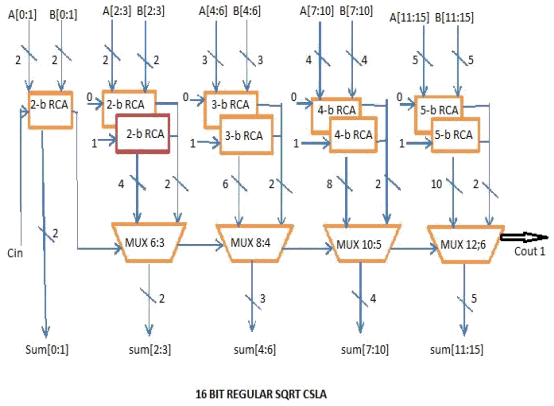
Full Adder Truth Table

CARRY IN	*input B*	*input A*	*CARRY OUT*	*SUM digit*
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

ARCHITECTURE OF REGULAR SQRT CSLA:

REGULAR 16 BIT SQRT CSLA:

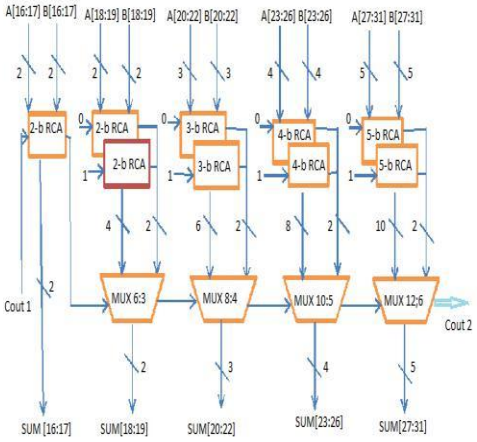
The Regular 16-bit SQRT CSLA is implemented using the two blocks of Ripple Carry Adders. First block of the Ripple Carry Adder has an carry input of Cin=1 and the second block of Ripple Carry Adders has the carry input cin=0. The output from the second block of the Ripple Carry Adders is fed into the Multiplexers (MUX) and the sum and the carry. In Regular CSLA there is only one RCA is present to perform the least significant addition RCA[1:0], the other RCA perform calculation twice one time with the assumption of the carry being zero cin=0 and carry being one cin=1. Then the final output is drawn from the multiplexer.



16 BIT REGULAR SQRT CSLA

REGULAR 32 BIT SQRT CSLA:

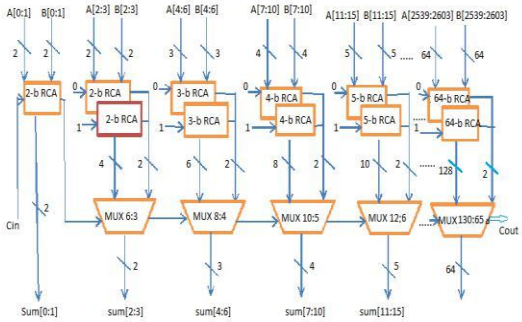
When the two blocks of Regular 16-bit SQRT CSLA is combined together to form the 32-bit Regular CSLA. Since the output from the 16-bit Regular SQRT CSLA is fed as carry input to the 32-bit Regular SQRT CSLA.



32 BIT REGULAR SQRT CSLA

REGULAR 64-BIT SQRT CSLA:

When the two blocks of 32-bit Regular SQRT CSLA is combined together forms the 64-bit Regular SQRT CSLA. The carry output from the 32-bit Regular CSLA is fed as carry input to 64-bit Regular CSLA and the total output is finally fed to the Multiplexer to get the sum and carry of 64-bits.



REGULAR 128-BIT SQRT CSLA:

When the two blocks of 64-bit Regular SQRT CSLA is combined together forms the 128-bit Regular SQRT CSLA. The carry output from the 64-bit Regular CSLA is fed as carry input to 128-bit Regular CSLA and the total output is finally fed to the Multiplexer to get the sum and carry of 128-bits.

DELAY AND AREA OF REGULAR 128-BIT SQRT CSLA:

From analysis the power consumption of Regular 128-bit SQRT CSLA is very low when compared to the 64-bit Regular CSLA. The performance of the 128-bit CSLA is also increased when compared to the 64-bit Regular CSLA but with a small speed penalty. Here the various bits of the Regular SQRT CSLA comparisions are given below.

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	57	66,560	
Number of occupied Slices	32	33,280	
Number of Slices containing only related logic	32	32	1
Number of Slices containing unrelated logic	0	32	
Total Number of 4 input LUTs	57	66,560	

```
Maximum combinational path delay: 17.722ns
```

Regular 16-bit SQRT CSLA

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	113	66,560	1%
Number of occupied Slices	63	33,280	1%
Number of Slices containing only related logic	63	63	100%
Number of Slices containing unrelated logic	0	63	0%
Total Number of 4 input LUTs	113	66,560	1%
Number of bonded IOBs	100	633	15%
Average Fanout of Non-Clock Nets	2.73		

```
Maximum combinational path delay: 26.819ns
```

Regular 32-bit SQRT CSLA

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	223	66,560	1%
Number of occupied Slices	121	33,280	1%
Number of Slices containing only related logic	121	121	100%
Number of Slices containing unrelated logic	0	121	0%
Total Number of 4 input LUTs	223	66,560	1%
Number of bonded IOBs	196	633	30%
Average Fanout of Non-Clock Nets	2.71		

```
Maximum combinational path delay: 44.972ns
```

Regular 64-bit SQRT CSLA

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	442	66,560	1%
Number of occupied Slices	239	33,280	1%
Number of Slices containing only related logic	239	239	100%
Number of Slices containing unrelated logic	0	239	0%
Total Number of 4 input LUTs	442	66,560	1%
Number of bonded IOBs	386	633	60%
Average Fanout of Non-Clock Nets	2.72		

```
Maximum combinational path delay: 81.909ns
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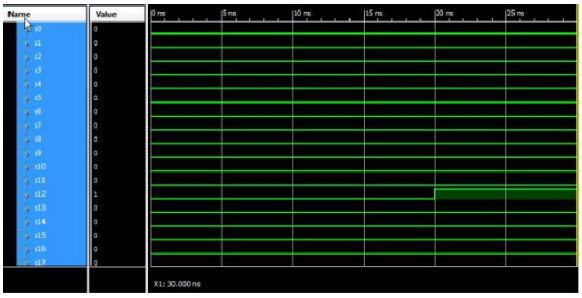
Regular 128-bit SQRT CSLA

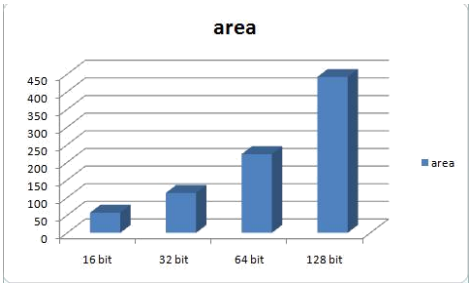
SIMULATION RESULTS:

The simulation result shows the Regular 128-bit SQRT CSLA consumes the low power and has an increased performance than the 64-bit regular SQRT CSLA. The idea was implemented in the Xilinx ISE software and the results are simulated. The simulation results show the reduction in power with the increase of number of bits of Ripple Carry Adder. The total power consumed is only 0.338 watts.

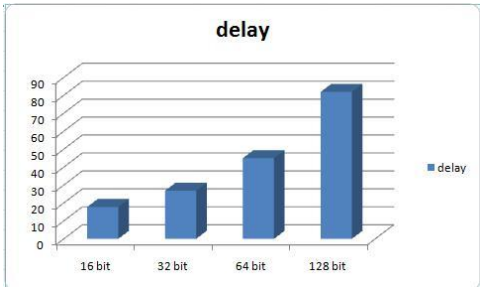


	Total	Dynamic	Quiescent
Supply Power (W)	0.338	0.000	0.338

From the area analysis graph it is observed that the area of the Regular SQRT CSLA decreases with the increase in the number of bits. Processing speed of the system also increased. It does challenging task better than other combinational circuits.



From the delay analysis, when the number of bits increases the power consumption of the regular SQRT CSLA increases with small time penalty.



CONCLUSION:

Modified architecture is using BEC. It increases the area, which is the major disadvantage. The architecture is proposed to overcome the above disadvantage by using ripple carry adder. It reduces area than the conventional and modified Square root Carry select adder. From the analysis of area and delay graph, the delay is increased slightly with the increase in number of bits of CSLA, but there is a reduction in the area. The total RAM used for this process is also low when compared to the other CSLA's. The idea of our work was implemented in the Xilinx ISE software.

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MANIKANDAN.A pursuing B.E. 3rd year Electronics and Communication Engineering at SNS College of Technology, Coimbatore. His area of interest are microprocessor design, VLSI system implementation, image processing.

LOKESHWARAN.R pursuing B.E. 3rd year Electronics and Communication Engineering at SNS College of Technology, Coimbatore. His area of interest are circuit designing, automation.

MATHIALAGAN.P pursuing B.E. 3rd year Electronics and Communication Engineering at SNS College of Technology, Coimbatore. His area of interest are optical and photonics, Robotics and PCB designing and PIC programming.

PRABHAKARAN.K pursuing B.E. 3rd year Electronics and Communication Engineering at SNS College of Technology, Coimbatore. His area of interest are embedded C programming, VLSI designing, image processing.