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Area and Power Efficient Hybrid Reversible Shift Register

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***Abstract*— Reversible logic has emerged as a most important area of research due to its ability to reduce the power dissipation which is the major requirement in low power digital circuit designs. In this paper an area and power efficient 8T reversible D-flip flop design and 32 transistor 4-bit reversible shift register has been presented by hybridizing PTL and GDI techniques. The GDI logic is used in this design implementation because GDI technique allows reducing the power consumption, area and delay. The PTL technique also reduces the area. In this paper GDI and PTL techniques are combined to design the reversible shift register. The FRG and FG gates are used to design the proposed reversible D-flip flop and proposed reversible shift register. Schematic diagrams are drawn in DSCH2 and simulations are run on Microwind3.1 design tool using 180nm technology file. Also the simulation of layout and parametric analysis has been done for the proposed reversible D-flip flop and proposed reversible shift register design. Results show that area consumed by the proposed hybrid reversible shift register is 2210.3μm^2 on 180nm technology. At 1.2V input supply voltage the proposed shift register has shown an improvement of 76.95% in power on 180nm technology.**

***Index Terms* — GDI, PTL, Reversible logic, Microwind, Low power VLSI, CMOS design.**

I. INTRODUCTION

Shift registers are relatively important timing circuits, commonly used in digital circuits. Shift registers are not only used to store information, but also used for the serial and parallel data transformation, signal transmission delays, data processing and data computing, so the study of the shift register are of great significance [1]. The conventional, complementary metal oxide semiconductor circuits use direct current power supply, the energy always converts from electrical energy into heat in an irreversible form, resulting in non-energy recovery. Although reducing node capacitances, supply voltage, and switching activity are used to reduce power consumption, energy saving is limited [2]. Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching, and static power is consumed regardless of transistor switching [3]. In one complete cycle of CMOS logic, current flows from V_{DD} to the load capacitance to charge it and then flows from the charged load capacitance to ground during discharge. Therefore in one complete charge/discharge cycle, a total of $Q=C_LV_{DD}$ thus transferred from V_{DD} to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage [4]. Despite many advantages, CMOS suffers from increased area, more power dissipation and correspondingly increased capacitance and delay, as the logic gates become more complex [5]. All NMOS and PMOS transistors used in this circuit have the same W/L ratio. It is required to adjust the transistor dimensions individually to get optimized time domain performance of the circuit [6].

In irreversible logic some information about the inputs is erasing every time a logic operation is performed. Thus we cannot deduce the input from knowing the output alone [7]. Energy loss is an important issue in modern VLSI designs. Though the improvement in higher-level integration and the advancement of new fabrication processes have significantly reduced the heat loss over the last decades, physical limit exists in the reduction of heat [8]. According to R. Landauer's research in the 1960s, the amount of energy dissipated for every irreversible bit operation is given by KTln2, K is the Boltzmann's constant having the value $1.3807X10^{-23}$ JK^{-1}. T is the operating temperature. At room temperature the dissipating heat is around $2.8X10^{-21}$ J, which is small but non-negligible. Reversible logic does not erase the information, dissipate zero heat [9]. For a given system to be reversible, it has to be able to operate in backward direction. This ability allows us to reproduce input from only knowing the output. The C. H. Bennett in 1973 concluded that no energy would dissipate from a system as long as the system was able to return to its initial state of its final state [10]. Reversible logic is the logic supporting the process of running the system in the backward direction. Reversible logic circuits are also called lossless circuits, because neither information loss nor energy loss occurs in these logic circuits. The applications of reversible logic circuits are optical computing, nanotechnology, quantum computing, reversible memory circuits and ultra low power CMOS design [11].

Reversible logic have extensive applications in emerging technologies such as optical computing, quantum computing, quantum dot cellular automata as well as ultra low power VLSI circuits. Recently, several researchers have focused their efforts on the design and synthesis of efficient reversible logic circuits. In these works, the primary design focus has been on optimizing the number of reversible gates and the garbage outputs [12]. GDI technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors [13]

II. REVERSIBLE LOGIC

Some commonly used reversible logic gates are discussed as follows:

The Feynman gate is also called CNOT gate or the quantum XOR gate due to its popularity in the quantum computing. The Feynman gate is a reversible gate having 2 inputs and 2 outputs.

Figure 1. Feynman Gate (2 X 2)

The figure 1 shows the Feynman gate. The Feynman gate is completely reversible, that is, the circuit can also work for reverse operation. In figure 1 input P serves as a control input. In forward calculation, the X=P, if P=0 then Y is the duplicate copy of input Q. If P=1 then o/p Y is the inverse of Q. In reverse calculation, P=X, if X=0 then Q=Y else Q is the inverse of Y. For this reason, the Feynman gate is also called the controlled NOT (CNOT) gate.

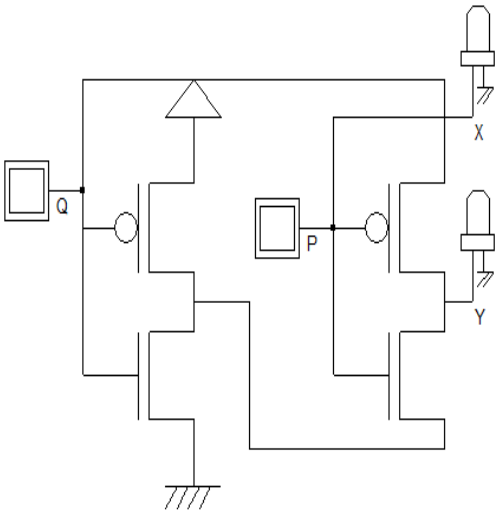

Figure 2. Transistor Realization of Feynman Gate

The figure 2 shows the proposed transistor implantation of Feynman gate using only four transistors. The logic style used for the realization is the gate diffusion input. The quantum cost of every 2 X 2 gate is the same and the cost is 1. This proposed gate is used in the realization of reversible shift register.

This gate is most widely used reversible logic gate. The Fredkin gate is reversible 3 X 3 logic gate because it has 3 inputs and 3 outputs. The 3 inputs are A, B, C and the 3 outputs are X, Y, Z. In the Fredkin gate X=A, Y=ĀC+AB and Z=ĀB+ AC. The output X is the copy of input A. The Fredkin gate and Feynman gate are used to construct reversible D flip-flop. The quantum cost of FG gates is 5.

Figure 3. Fredkin Gate (3 X 3)

The Fredkin gate uses A as a control input. In forward computation X=A, if A=0 then Y is the copy of input B and Z is the copy of input. If A = 1, then the output Y is the copy of input C and Z is the copy of input B. In backward computation, A=X, if X=0 then B is the copy of Y and C is the copy of Z. If X=1 then C is the copy of Y and B is the copy of Z.

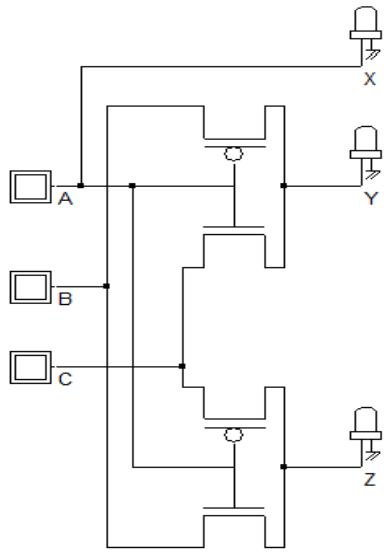

Figure 4. Transistor Realization of Fredkin Gate

The figure 4 shows the transistor implementation of the Fredkin gate. The four transistors are used to implements the Fredkin gate.

The Sayem gate is the 4X4 gate this gate has four inputs and four outputs. The four inputs are A, B, C, D and four outputs are W, X, Y, Z.

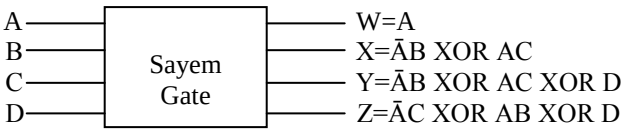

Figure 5. Sayem Gate (4 X 4)

The first output W is the copy of the input A. The input A is the control input of the Sayem gate [14].

The figure 6 shows the transistor implementation of the Sayem gate. The forty two transistors are required to implements the Sayem gate.

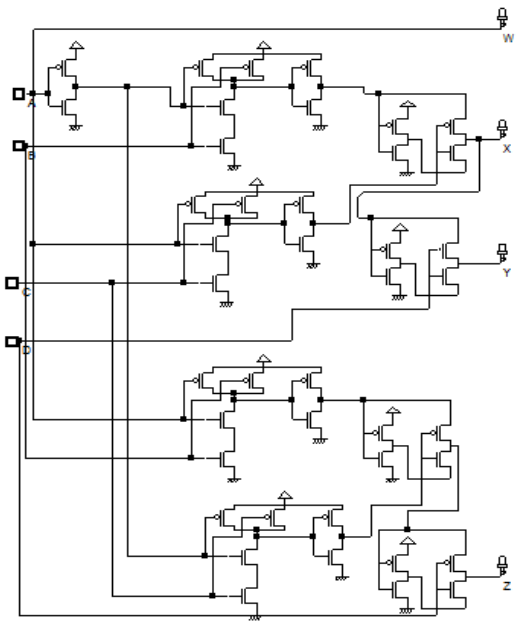

Figure 6. Transistor Realization of Sayem Gate

III. PROPOSED REVERSIBLE SHIFT REGISTER

A flip-flop is a bi-stable electronic circuit that has two stable states and can be used as a one-bit memory device. The characteristic equation of the D flip flop is $Q^+ = D.CLK+Q.\overline{CLK}$, where Q^+ is the next state of the D flip-flop. The reversible D flip flop is implemented by using the Fredkin gate and Feynman gate. The Fredkin gate in the figure 4 has 3 inputs CLK, D and the third input is the feedback from the output of the Feynman gate. The first output of Fredkin gate is the CLK output. The second output of the Fredkin gate is the garbage output, which is not used. The third output of the Fredkin gate is fed to the first input of the Feynman gate. The second input of the Feynman gate is always 0.

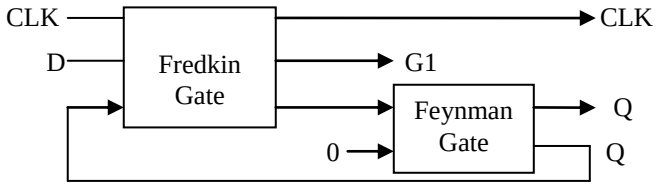

Figure 7. Reversible D Flip-Flop

The first output of Feynman gate is the Q and the second output is connected to the third input of the Fredkin gate. Proposed reversible D-flip flop has been implemented by using only 8 transistors which provide an area efficient design as compared to existing designs of reversible D-flip flops.

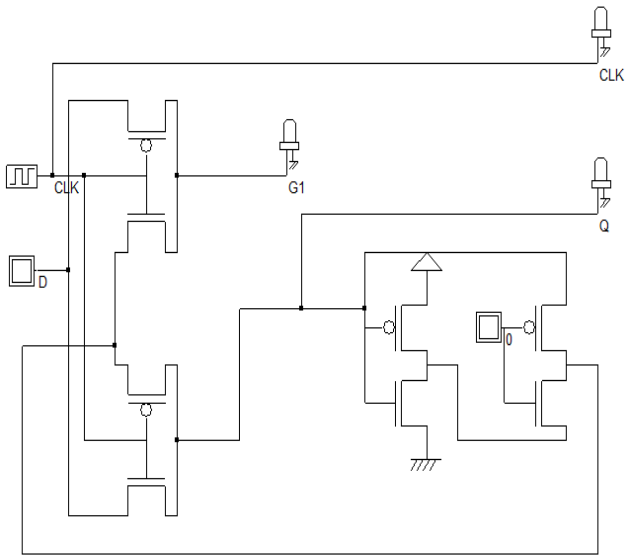

Figure 8. Proposed Hybrid Reversible D-Flip Flop

The figure 8 shows the design of reversible D flip-flop which is designed by using the FG & FRG gates. Proposed reversible D flip flop has been compared with existing design in terms of area in microwind designing tool. Microwind deals with both front end and back end designing. In front end it has DSCH in which both transistor level and gate level designing can be done.

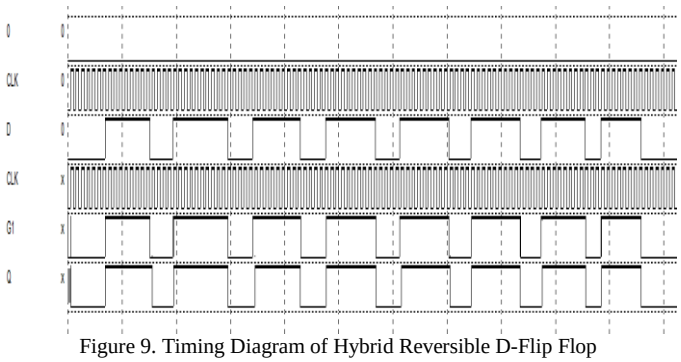

Figure 9. Timing Diagram of Hybrid Reversible D-Flip Flop

The figure 9 shows the timing simulation of hybrid reversible D-flip flop. Verification and simulation of the functionality of proposed reversible D flip flop is first done by using DSCH 2 designing tool. DSCH generate a verilog file which can be compiled by the Microwind back end designing tool to get power and area consumption. Proposed reversible D-flip flop is compared with the existing design in terms of area on 180nm technology. GDI technique is a power and area efficient technique for designing digital circuits as compared to PTL, TG and CPL.

The shift register is one of the most extensively used functional devices in digital systems. A shift register consists of an array of flip-flops connected together so that information bits can be shifted one position to either right or left depending on the design of the device. The shift registers are also used as a buffer circuit. The reversible shift registers are used to construct the Quantum computers. The serial in the serial output shift register (SISO) is the simplest shift register. The 4 bit reversible shift registers is implemented by using 4 reversible D flip-flops which is designed by using the Fredkin gate and Feynman gate. The area consumed by this shift register is less as compare to the reversible shift register designed by the reversible D flip-flops using Sayem gate. The serial input is entered in the first flip-flop and serial output appears at the last flip flop. This shift register is called serial in serial out shift register because the input is entered in serial manner and output is also appears in serial form.

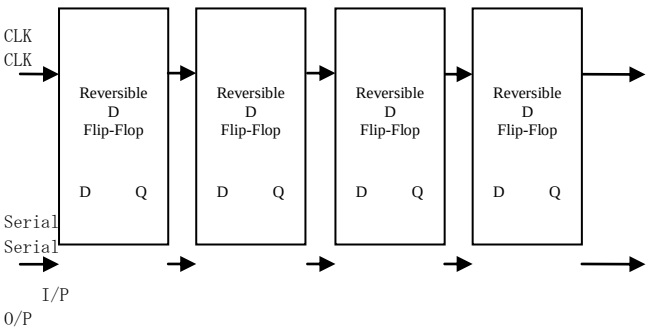

Figure 10. 4-bit Hybrid Reversible SISO Shift Register

This design consists of 4 Fredkin gates and 4 Feynman gates. The data output of one flip-flop is the data input of next flip-flop.

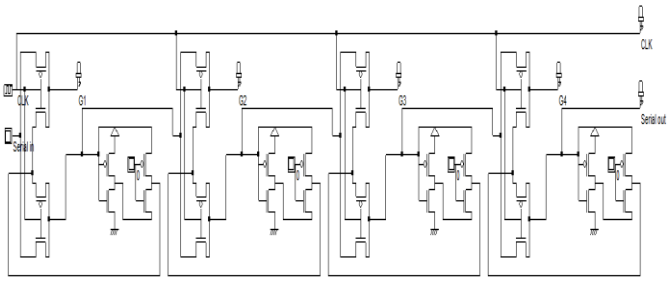

Figure 11. 4-bit Hybrid Reversible SISO Shift Register

The figure 11 shows the hybrid 4-bit reversible shift register which consists of 32 transistors. The schematic is designed and verified in DSCH design tool and area and power consumption of the proposed reversible shift register is calculated in Microwind back end designing tool.

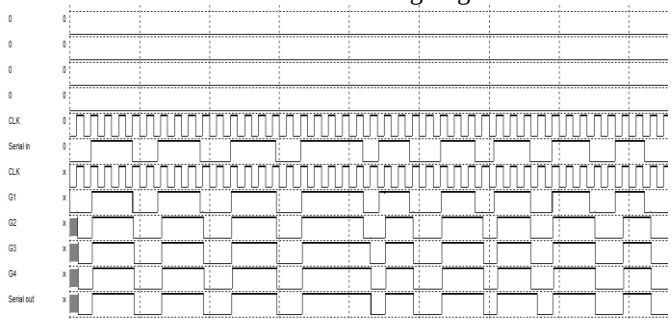

Figure 12. Timing Diagram of Hybrid Reversible SR

The figure 12 shows the timing simulation of hybrid reversible 4-bit shift register. Timing simulation shows the exact functionality of Hybrid reversible SR. Proposed hybrid reversible shift register is compared with the existing design in terms of area on 180nm technology.

IV. LAYOUT DESIGN ANALYSIS

For complex circuits it becomes very difficult to conduct the manual layout so automatic layout generation approach is preferred. Before the layout simulation, the schematic diagram has been designed in the DSCH design tool. After the schematic diagram the verilog file is generated in the DSCH design tool. This verilog file is understandable by the Microwind to construct the layout with exact desired design rules. The other way to create the layout is by PMOS and NMOS devices using cell generator provided by the Microwind.

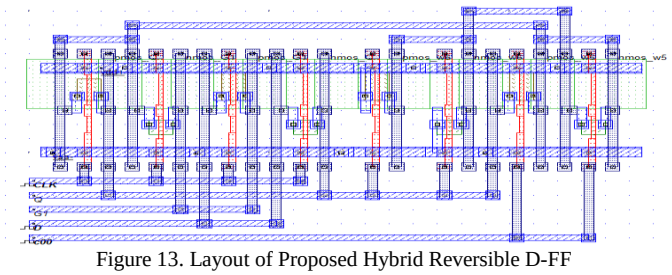

Figure 13. Layout of Proposed Hybrid Reversible D-FF

The figure 13 shows the layout of hybrid reversible D-flip flop at 180nm technology in Microwind back end design tool.

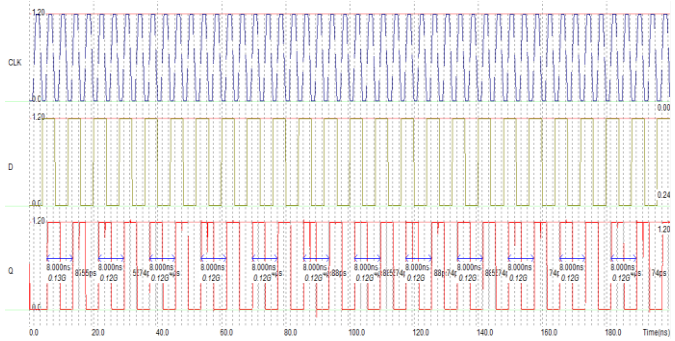

Figure 14. Analog Simulation of Proposed Hybrid D-FF

The analog simulation is done Microwind back end design tool. The analog simulation has been carried out to know the power consumption at different temperatures and voltages. Analog simulation is carried out for proposed reversible D-flip flop at 180nm technology.

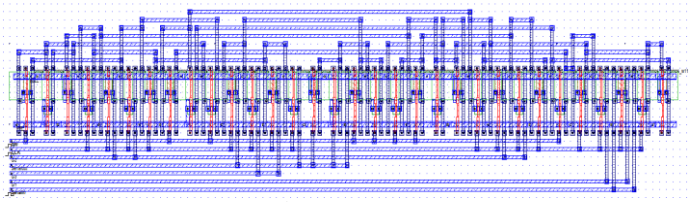

Figure 15. Layout of Proposed Hybrid Reversible SR

The figure 15 shows the layout of the hybrid reversible shift register at 180nm technology. This layout is generated automatically in Microwind back end design tool by using the verilog file which is generated in DSCH design tool.

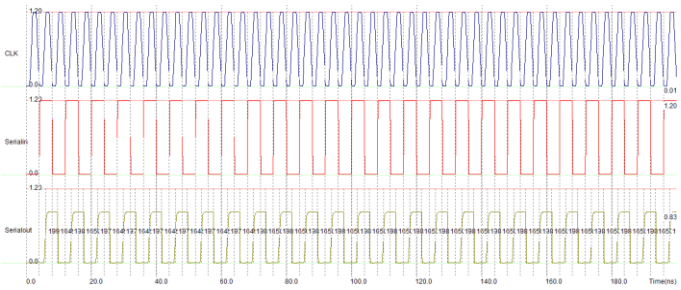

Figure 16. Analog Simulation of Proposed Hybrid SR

The analog simulation for the proposed reversible SR has been carried out to know the power consumption at different temperatures and voltages. Analog simulation is carried out for proposed reversible shift register at 180nm technology.

V. RESULTS & DISCUSSIONS

The performance of proposed hybrid shift register has been carried out in terms of power and area on 180nm technology. Simulation has been performed using Microwind back end design tool. Results are measured in terms of variation in power with respect to the variation in temperature and voltage. Comparative analysis of proposed reversible D-flip flop in terms of area and power with other existing reversible D-flip flop has been shown in Table I.

Table I. Comparison of Existing & Proposed D Flip-flop

Parameter	Reversible D FF using CMOS[1]	Proposed Reversible Hybrid D-flip flop
Area	2848.7μm^2	428.3μm^2
Power	0.262mW	0.058mW

The table I shows that the reversible D flip-flop designed by hybrid technique consume less area as compared to the reversible D flip-flop designed by CMOS. In this paper, we use the reversible D flip-flop which is designed by using FRG and FG gates to construct the 4-bit reversible shift register that is area efficient as compared to existing reversible shift register.

Table II. Power Variation with Supply Voltage in FFs

V_{DD} (V)	Power (mW)	
	D-FF using AS & FG Gate by CMOS [1]	Proposed Hybrid D-FF using FRG & FG Gate
0.2	0.009	0.001
0.4	0.017	0.001
0.6	0.017	0.002
0.8	0.081	0.006
1	0.115	0.007
1.2	0.124	0.009
1.4	0.163	0.011
1.6	0.193	0.015
1.8	0.238	0.026

The variation in power with the supply voltage at 180nm is given in the table II. This table shows that the power variation with supply voltage is less in the proposed design as compare to the existing design.

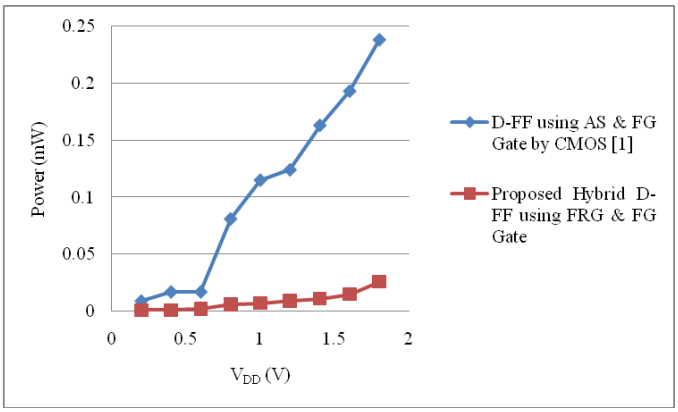

Figure 17. Power Variation with Supply Voltage

The graph in the figure 17 shows the variation in power with supply voltage at 180nm technology. The variation in power with respect to supply voltage is less in the proposed design as compare to the existing design.

Table III. Power Variation with Temperature in FFs

t°	Power (mW)	
	Reversible D-FF by CMOS [1]	Proposed Hybrid reversible D-FF
20	0.262	0.060
40	0.264	0.056
60	0.266	0.053
80	0.269	0.05
100	0.273	0.048
120	0.277	0.046
(Temp. Coef.)TC=0.0 mV/°C		

The variation in power with the temperature of reversible D-flip flop at 180nm is given in the table III. This table shows that the power variation with temperature is less in the proposed design as compare to the existing design.

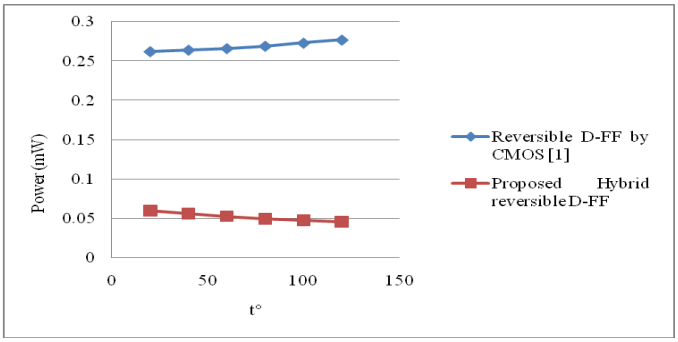

Figure 18. Power Variation with Temperature

The graph in the figure 18 shows the variation in power with temperature at 180nm technology. The variation in power with respect to temperature is less in the proposed design as compare to the existing design.

Comparative analysis of proposed reversible shift register in terms of area and power with other existing reversible shift register has been shown in Table IV.

Table IV. Comparison of proposed SR with existing SR

Parameter	Reversible SR uses CMOS [1]	Proposed Hybrid reversible shift register
Area	14466.5μm^2	2210.3μm^2
Power	2.314mW	0.284mW

The table IV shows that the reversible shift register designed by combining the GDI and PTL technique consume less area and power as compared to the reversible shift register designed by CMOS.

Table V. Power Variation with Supply Voltage in SRs

V_{DD}(V)	Power(mW)	
	Reversible SR by CMOS [1]	Proposed Hybrid reversible SR
0.2	0.064	0.001
0.4	0.007	0.003
0.6	0.077	0.016
0.8	0.128	0.038
1	0.272	0.049
1.2	0.282	0.065
1.4	0.871	0.069
1.6	1.202	0.105
1.8	2.011	0.184

The variation in power with the supply voltage of reversible shift register at 180nm is given in the table V. This table shows that the power variation with supply voltage is less in the proposed design as compare to the existing design.

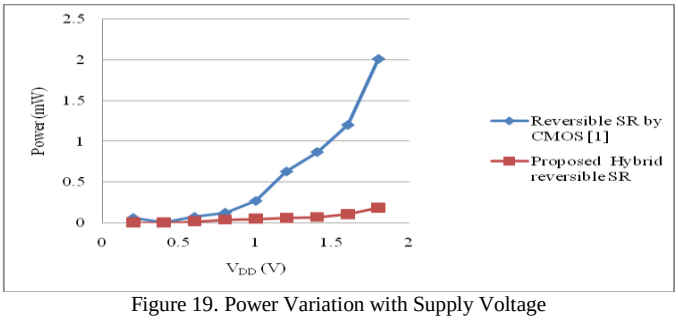

Figure 19. Power Variation with Supply Voltage

The graph in the figure 19 shows the variation in power with supply voltage at 180nm technology. The variation in power with respect to supply voltage is less in the proposed design as compare to the existing design.

Table VI. Power Variation with Temperature in SRs

t°	Power (mW)	
	Reversible SR by CMOS [1]	Proposed Hybrid reversible SR
20	1.578	0.289
40	1.656	0.276
60	1.730	0.265
80	1.801	0.256
100	1.871	0.249
120	1.940	0.243
(Temp. Coef.)TC=0.0 mV/°C		

The variation in power with the temperature of reversible shift register at 180nm is given in the table VI. This table shows that the power variation with temperature is less in the proposed design as compare to the existing design.

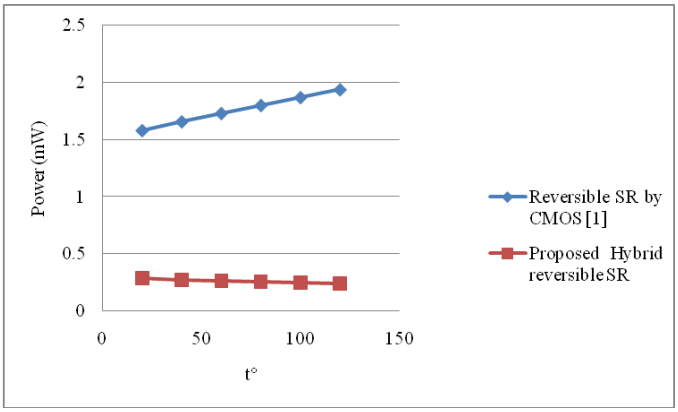

Figure 20. Power Variation with Temperature

The graph in the figure 20 shows the variation in power with temperature at 180nm technology. The variation in power with respect to temperature is less in the proposed design as compare to the existing design.

VI. CONCLUSION

An alternative 4-bit hybrid reversible shift register is designed by using FRG and FG gates and hybridized GDI and PTL techniques. The proposed reversible shift register is implemented by 32 transistors. A new area efficient reversible D-flip flop is implemented by using only 8 transistors. Proposed reversible D-flip flop consumes 428.3μm^2 area at 180nm. Proposed reversible D-flip flop has been also compared in terms of area from other existing reversible D-flip flop and proposed reversible D-flip flop has been proven area efficient as compared to other. This reversible D-flip flop has been used as a basic module in proposed hybrid reversible shift register. Area and simulation of proposed shift register has been shown on 180nm technology. Area of proposed design is 2210.3μm^2 on 180nm technology. At 1.2V input supply voltage the proposed hybrid shift register has shown an improvement of 76.95% in power on 180nm technology. The proposed design has the applications to build reversible memory circuits. This paper forms an important step in the building of complex reversible sequential circuits for building quantum computers.

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