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An efficient low power dual dynamic node Hybrid flip-flop with self controllable Voltage level circuit

Velumani.V[1] , Kowsalya. T[2]
Post Graduate Scholar[1], Associate Professor[2]
United Institute of Technology, Coimbatore

Abstract:**Flip-flops are critical timing elements in digital circuits which have a large impact on circuit speed and power consumption in VLSI circuits. A Low power high performance dual dynamic node hybrid flip-flop and embedded logic module WITH SVL Circuit is DESIGNED. The proposed design eliminates large capacitance present in the precharge node of several state of the art designs following a split dynamic node structure that separately drives the output pull-up and pull-down transistors. The proposed designs reduce the pipeline overhead and power delay product. The performance comparisons made in 0.18um technology using tanner EDA7.0 shows a power reduction of 38.5% compare to DDFF & 83.1% compare to DDFF-ELM, with no degradation in speed performance. On the other hand, the speed remains almost constant in terms of the switching the input signal by adding "Self-controllable Voltage Level (SVL)" Circuit. The result of the simulation demonstrates that this DDFF&DDFF-ELM with SVL Circuit is a viable means to improve design performance, operating speed and achieve the greater power efficiency.**

Key Words:Embedded Logic, Flip-Flops, high speed, low-power, SVL circuit

I. INTRODUCTION

The tremendous advancements in VLSI technologies in the past few years have fuelled the need for intricate tradeoffs among speed, power dissipation and area. With gigahertz range microprocessors becoming common place along with the perennial increments in power dissipation, the emphasis is even more on pushing the speeds to their extreme while minimizing power dissipation and die area. The tremendous advancements in VLSI technologies in the past few years have fuelled the need for intricate tradeoffs among speed, power dissipation and area. With gigahertz range microprocessors becoming common place along with the perennial increments in power dissipation, the emphasis is even more on pushing the speeds to their extreme while minimizing power dissipation and die area. The advancements has made speed area unit continually moving forward, from low scale integration to massive and VLSI and from MHz (MHz) to rate (GHz). The system necessities are rising up with this continuous advancing method of technology and speed of operation. In synchronous systems, high speed has been achieved exploitation advanced pipelining techniques. In fashionable deep-pipelined architectures, pushing the speed additional up demands a lower pipeline overhead. This overhead is that the latency related to the pipeline elements, like the flip-flops and latches. Intensive work has been dedicated to improve the performance of the flip-flops within the past few decades. Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes. There are basically four main types of latches and flip-flops: SR, D, JK, and T.The major differences in these flip-flop types are the number of inputs they have and how they change state. For each type, there are also different variations that enhance their operations.The D Flip-Flop Latches are often called level-sensitive because their output follows their inputs as long as they are enabled.They are transparent during this entire time when the enable signal is asserted. There are situations when it is more useful to have the output change only at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. Thus, we can have all changes synchronized to the rising or falling edge of the clock. There have been many methods proposed to eliminate the drawback of power consumption and latency. Transmission gate flip-flop is a method which have a fully static master slave structure by cascading two identical pass-gate latches and provides a short clock to output latency. This flip-flop is realized by using two transmission gate based latches operating on Complementary clocks. Several varieties of the transmission gate based are available. PowerPC 603 flip-flop has a structure and it is a combination of TGMS flip-flop and mC²MOS flip-flop. The feedback transmission gate is changed with a clocked inverter. This flip-flop is realized by using two transmission gate based latches operating on complementary clocks. Hybrid Latch Flip Flopstructure is basically a level sensitive latch which is clocked with an internally generated sharp pulse. This

sharp pulse is generated at the positive edge of the clock using clock and delayed version of clock.Semi Dynamic Flip Flop structure has been denoted a semi dynamic flip-flop(SDFF) because of its combination of dynamic and staticcircuits.Cross Charge Control Flip Flop large precharge-capacitance in a wide variety of designs results from the fact that both the output pull-up and the pull-down transistor are driven by this precharge node.Dual Dynamic Node Hybrid Flip-Flop architecture has Node *X*1 is pseudo-dynamic, with a weak inverter acting as a keeper, whereas, compared to the XCFF, in the new architecture node *X*2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF. Semi Dynamic Flip-Flop Embedded LogicModuleThe major advantage of the SDFF is the capability to incorporate complex logic functions efficiently. The efficiency in terms of speed and area comes from the fact that an *N*-input function can be realized in a positive edge triggered structure using a pull-down network (PDN) consisting of *N* transistors. Dual Dynamic Node Hybrid Flip-Flop Embedded Logic Module has a revised structure of the dual dynamic node hybrid flip-flop with logic embedding capability (DDFF-ELM) the revised model, the transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed.Though there are several proposed methods to reduce the power consumption each face its own drawback. Here we propose a new model of reducing power consumption which utilizes The SVL (Self Controllable Voltage Level Circuit) circuit. This considerably reduces the power consumption when compared to the other existing techniques. The paper is organized as follows. Section 2 discusses about the Existing approach used. Section 3 is devoted to the proposed methods. Section 4 deals with Results and graphs. Section 5 deals with conclusion and Future Enhancements.

II. EXISTING METHODS

The Existing method utilizes two different methods and they are dual dynamic node hybridflip-flop (DDFF) and a novel embedded logic module (DDFFELM). They are compared along with XCFF method. Their new designs proved to be free from unwanted transitions resulting whenthe data input is stable at zero. The other method DDFF-ELM presents a speed,area, and power efficient method to reduce the pipeline overhead.

Dual Dynamic Node Hybrid Flip-Flop (DDFF)

The large precharge-capacitance in a wide variety of designs results from the fact that both the output pull-up and the pull-down transistor are driven by this precharge node. These transistors being driving large output loads contribute to most of the capacitance at this node. This common drawback of many conventional designs was considered in the design of XCFF. It reduces the power dissipation by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors as shown in Fig.2.1. Since only one of the two dynamic nodes is switched during one CLK cycle, the total power consumption is considerably reduced without any degradation in speed. Also XCFF has a comparatively lower CLK driving load. One of the major drawbacks of this design is the redundant precharge at node *X*2 and *X*1 for data patterns containing more 0 s and 1 s, respectively. In addition to the large hold time requirement resulting from the conditional shutoff mechanism, a low to high transition in the CLK when the data is held low can cause charge sharing at node *X*1. This can trigger erroneous transition at the output unless the inverter pair INV1-2 is carefully skewed. This effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design.

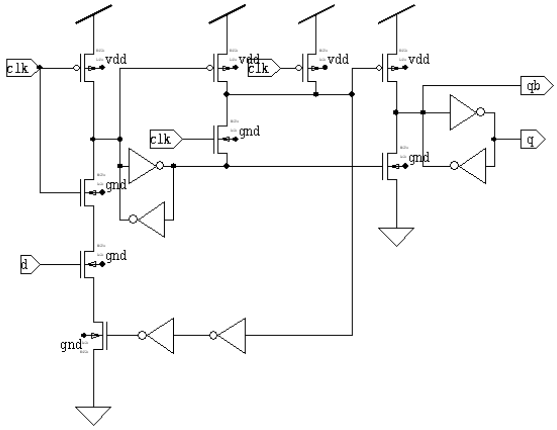

Fig.2.1 Schematic diagram of XCFF

The XCFF has a single data-driven transistor; embedded logic. XCFF is not very efficient due to the susceptibility to chargesharing at the internal dynamic nodes. The proposed DDFF architecture of Node *X*1 is pseudo-dynamic, with a weak inverter acting as a keeper, whereas, compared to the XCFF, in the new architecture node *X*2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF.

The operation of the flip-flop can be divided into two phases:

1) The evaluation phase, when CLK is high, and
2) The precharge phase, when CLK is low.

The actual latching occurs during the 1–1 overlap of CLK and CLKB during the evaluation phase. If *D* is high prior to this overlap period, node *X*1 is discharged through NM0-2. This switches the state of the cross coupled inverter pair INV1-2 causing node *X*1*B* to go high and output *QB* to discharge through *NM*4. The low level at the node *X*1 is retained by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs. Thus, node *X*2 is held high throughout the evaluation period by the pMOS transistor *PM*1. As the CLK falls low, the circuit enters the precharge phase and node *X*1 is pulled high through *PM*0, switching the state of INV1-2. During this period node *X*2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node *QB* and maintain their voltage levels through INV3-4

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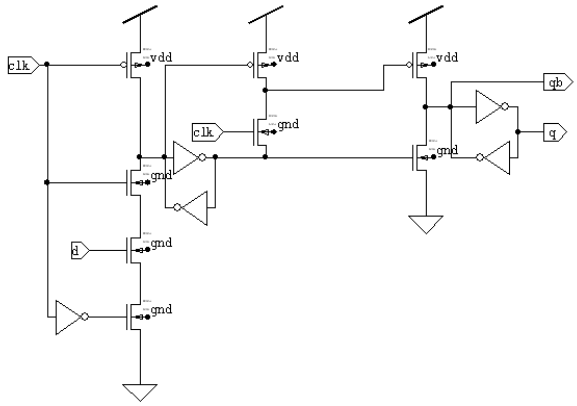


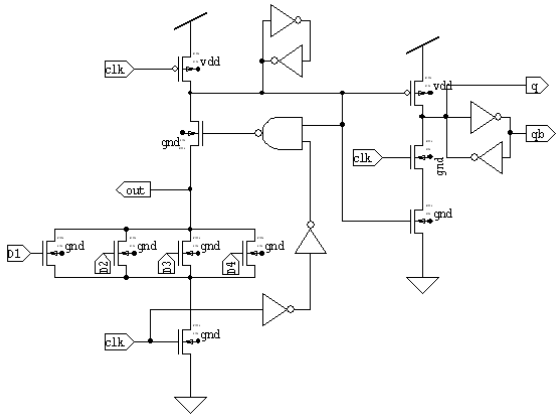
Fig.2.2 Schematic diagram of DDFF

If *D* is zero prior to the overlap period, node *X*1 remains high and node *X*2 is pulled low through *NM*3 as the CLK goes high. Thus, node *QB* is charged high through *PM*2 and *NM*4 is held off. At the end of the evaluation phase, as the CLK falls low, node *X*1 remains high and *X*2 stores the charge dynamically. The architecture exhibits negative setup time since the short transparency period defined by the 1–1 overlap CLK of and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low. Node *X*1 undergoes charge sharing when the CLK makes a low to high transition while *D* is held low. This result in a momentary fall in voltage at node *X*1, but the inverter pair INV1-2 is skewed properly such that it has a switching threshold well below the worst case voltage drop at node *X*1 due to charge sharing. The timing diagram shows that node *X*2 retains the charge level during the precharge phase when it is not driven by any transistor. Note that the temporary pull down at node *X*2 when sampling a "one" is due to the delay between *X*1 and *X*1*B*. The setup time and hold time of a flip-flop refers to the minimum time period before and after the CLK edge, respectively where the data should be stable so that proper sampling is possible. Here setup time and the hold time depend on the CLK overlap period.

Semi Dynamic Flip-Flop Embedded Logic Module

The major advantage of the SDFF is the capability to incorporate complex logic functions efficiently. The efficiency in terms of speed and area comes from the fact that an *N*-input function can be realized in a positive edge triggered structure using a pull-down network (PDN) consisting of *N* transistors Compared to the discrete combination of *N* a static gate and a flip-flop, this embedded structure offers a very fast and small implementation.

Fig.2.3 Schematic diagram of SDFF-ELM



Although SDFF is capable of offering efficiency in terms of speed and area, it is not a good solution as far as power consumption is concerned. Not too many attempts have been made to design a flip-flop, which can incorporate logic efficiently in terms of power, speed and area. The double-pulsed set-conditional-reset flip-flop (DPSCRFF) is one of the flip-flops capable of incorporating logic. But this structure has an explicit pulse generator to generate two pulses from the global CLK, which can cause large power consumption even when there is no data transition. Also, the three inverter delay between the two pulses, p1 and p2, causes a direct path between supply rails and a large glitch at the output when the data input remains high for more than one CLK cycle. In addition, the highly asymmetric timing nature of the design and the large hold time requirements prevent it from being directly cascaded without the use of additional buffers. Another flip-flop design aiming at efficient logic embedding is presented. But the overlap based logic cell introduced is similar to the single-phase pulsed flip-flop mentioned. Since SDFF is proved to outperform this design, we consider SDFF with embedded logic for comparative purposes.

Dual Dynamic Node Hybrid Flip-Flop Embedded Logic Module

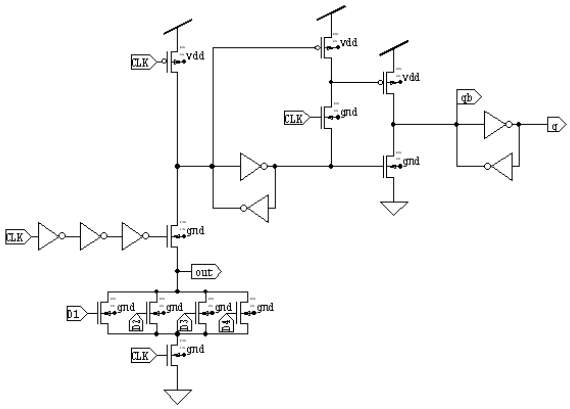


Fig.2.4. Schematic diagram of DDFF-ELM

The revised structure of the dual dynamic node hybrid flip-flop with logic embedding capability (DDFF-ELM) is shown in Fig. 2.4. Note that in the revised model, the transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed. The reason for this in clocking is the charge sharing, which becomes uncontrollable as the number of nMOS transistors in the stack increases. The same reason makes XCFF also incapable of embedding complex logic functions. In order to gets a clear picture of the charge sharing in XCFF it was simulated with different embedded functions and the amount of worst case charge sharing was calculated.

III. DUAL DYNAMIC NODE HYBRID FLIP-FLOP WITH SVL CIRCUIT

Design techniques for low-power circuits, for example, for use in battery-driven mobile phones, are not only needed for logic circuits (such as extremely fast addersand multipliers) but also for storage circuits (such asflip-flops, register files, and memories).There are two well-known techniques for reducing stand-by power. One is to use a multi-threshold voltage (MTCMOS) CMOS. This technique reduces P_{st} by disconnecting the power supply through the useof p-MOSFET switches (SWs) with higher thresholdvoltage (V). However, it has serious drawbacks such asthe need for additional fabrication processes for higher V_{th} and the fact that storage circuits based on thistechnique cannot retain data. The other techniqueinvolves using a variable threshold-voltage CMOS(VTCMOS) which reduces leakage current byincreasing substrate-bias (V).

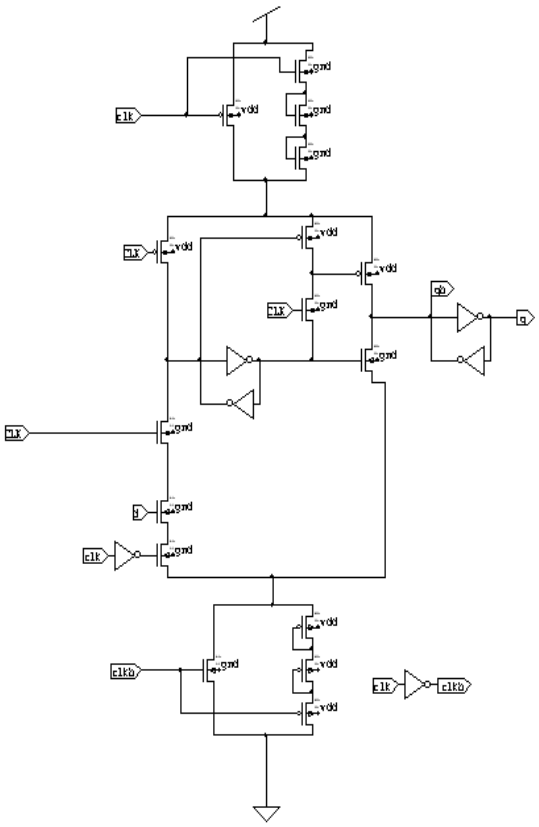


Fig.3.1 Schematic diagram of DDFF SVL Circuit

This technique also facessome serious problems, such as very slow substrate-biascontrolling operation, large area penalty, and large powerpenalty due to substrate-bias supply circuits. To solve the above-mentioned drawbacks, a self-controllable-voltage-level (SVL) circuit, which can significantly decrease P_{st} while maintaining high-speed performance, has been developed. The SVL (Self Controllable Voltage Level Circuit) circuit consists of an upper SVL (U-SVL) circuit and a lower SVL (L-SVL) circuit, where a Dual Dynamic node Hybrid Flip Flop has been used as the load circuit. The U-SVL circuit is constructed of an extensive channel pull-up pMOSFET switch (PSW) and multiple nMOSFET resistors connected in series. Similarly, the L-SVL circuit incorporates a wide channel pull-down nMOSFET switch (nSW) and multiple series-connected pMOSFET resistors (pRSm). The Type III SVL circuit along with DDFF & DDFF-ELM is shown in Figure 3.1 & 3.2. The upper SVL consists of a single p-MOSFET switch (p-SW) and m n-MOSFET switches (n-SW) Similarly, the lower SVL circuit consists of single n-MOSFET switch (n-SW) and m p-MOSFET switch connected in series.

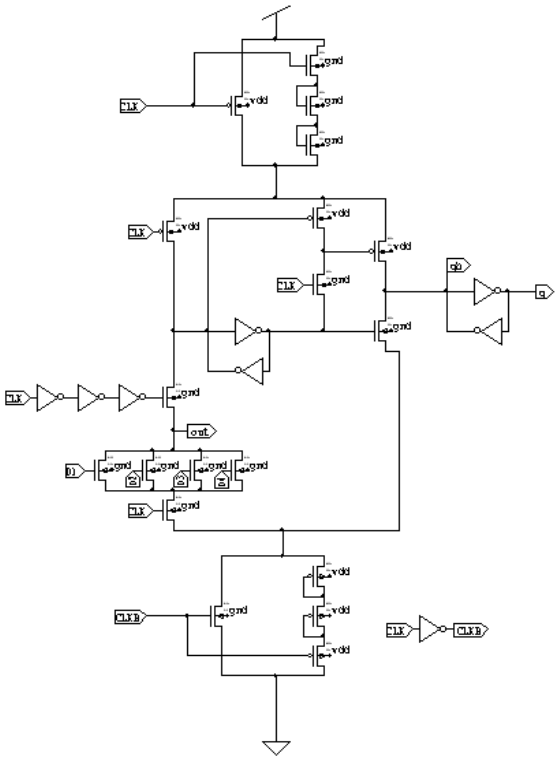


Fig.3.2 Schematic diagram of DDFF- ELM SVL circuit

The "on p-SW" connects a power supply (V_{DD}) and load circuit in active mode, and "on n-SW" connects V_{DD} and load circuit in standby mode. Similarly, the lower SVL circuit consists of single n-MOSFET switch (n-SW) and m p-MOSFET switch connected in series, is located between a ground level (V_{SS}) and the load circuit. The lower SVL Circuit not only supplies V_{SS} to the active load circuit through the "on n-SW" but also supplies V_{SS} to the standby load circuit through the use of the "on p-SWs". While the load circuit is active (i.e., CLKB="0" and CLK="1"), both the pSW and nSW are turned on, but the nRS1 and pRS1 are turned off. Therefore, the U-SVL and L-SVL circuits can supply a maximum supply voltage VD (=VDD) and a minimum ground-level voltage VS (=VSS=0), respectively, to the active load circuit. Thus, the operating speed of the load (proposed) circuit can be maximized.

IV. RESULTS AND COMPARISONS

The results are compared with the existing Technique. The tabulation of performance comparison of existing and proposed methods is shown below. The active device has considerably increased when compared to the proposed methods. The area of the proposed works has got comparatively increased with the existing methods.

Table I Tabulation Comparison

PARAMETERS	EXISTING METHODS		PROPOSED METHODS	
	DDFF	DDFF -ELM	DDFF SVL	DDFF -ELM SVL
ACTIVE DEVICES	18	25	28	35
AREA OF TRANSISTOR(μM^2)	792	1100	1232	1540
MAXIMUM POWER (mW)	1.559	2.635	1.174	1.804
POWER DELAY PRODUCT (nW per Sec)	31.19	13.18	5.871	9.027
ENERGY DELAY PRODUCT (fJ per Sec)	624	65.95	29.43	45.17
CURRENT (mw)	0.86	1.463	0.652	1.002

The Maximum power value has considerably reduced by 38.5% & 83% with the existing methods. The current value reduced efficiently in the proposed method.

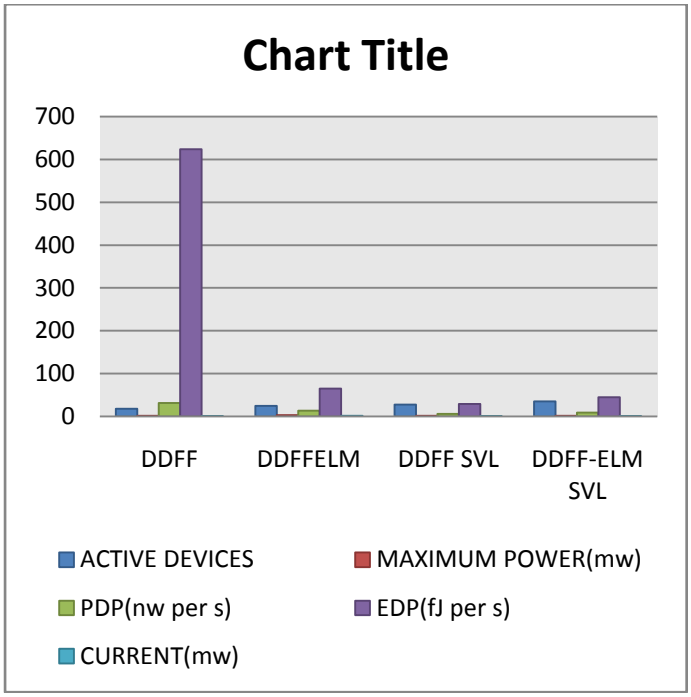


Fig 4.1 PERFORMANCE COMPARISION OF DDFF DDFFELM AND DDFFELM SVL METHODS

The power and delay calculation of DDFFSVL method is shown below. The calculation values are executed in Tanner software

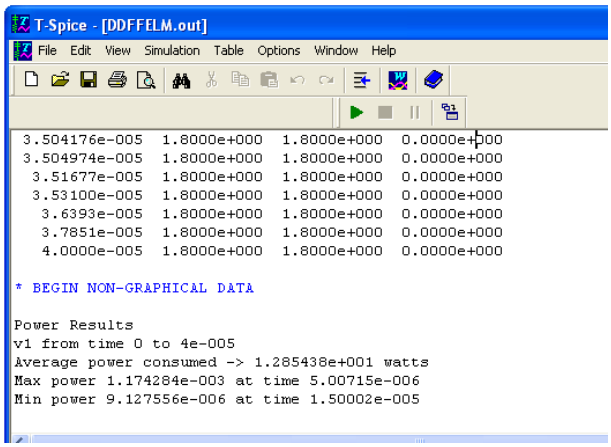


Fig.4.2 Power and Delay Calculation of DDFF SVL

The power and delay calculation of DDFF ELM SVL method is shown below The calculation values are executed in Tanner software

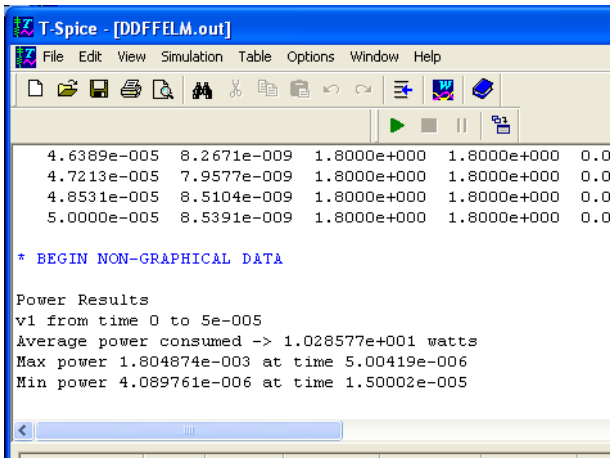


Fig.4.3Power and Delay calculation of DDFF-ELM SVL

The results and comparison of DDFF SVL and DDFF ELM SVL is Compared with the existing methods and it proves to be efficient than the existing methods.

V. CONCLUSION

The Proposed SVL Circuit consist of three modules comprising Upper Level SVL circuit controls the Vdd, lower level circuit controls the Gnd, and the DDFF acting as a load circuit.While the load circuits are in the active mode, the developed SVL circuit supplies the maximum DC voltages (*V*D and *V*S) to them through switches that are turned on. Thus, the load circuits can operate quickly. On the other hand, when the load circuits are in stand-by mode, it supplies slightly lower *V*D and relatively higher *V*S to them through "on SWs", so the drain-source voltages of the "off MOSFETs" in the stand-by load circuits decreases and *V*sub increases . Thus, *V*th increases and, consequently, sub threshold current decreases, so *P*st is reduced, while data are retained.Thus the overall advantages resulted in less PDP value and low power consumption than the existing methods. So DDFF-ELM SVL can be considered best logic design style with respect to all other existing flip-flops. From the above results, it is observed that DDFF-ELM SVL Circuit exhibits lowest DC power dissipation and comparable propagation delay by using SVL circuit design without trailing its performance. The idea can be extended for the further work to reduce the average power consumption and delay by using other modified techniques.

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