An Enhanced VLSI Architecture for 128x128 Vedic Multiplier using Modified Linear CSLA

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Abstract--A Carry-Select Adder(CSLA) is one of theway to implement an adder which is a logic element that computes the (n+1) bit sum of two n bit numbers in electronics.It is simple but fast,with a gate level depth of O(√n).Generally a CSLAconsists of two ripple carry adders and a multiplexer. The need in using CSLA is to reducearea by using efficient modification at gate level.Here 16 bit,32 bit,64 bit,modified linear CSLAis been developed and applied them into 16x16 bit, 32x32 bit,64x64 bit,128x128 bit vedic multiplier (VM) respectively. The regular CSLAconsumes more areaand hence modified linear CSLA is used which requires less area.For simulating the CSLA's and Vedic multipliers using CSLA's.ISIM simulator is used and synthesized through Xilinx Project Navigator 14.5.This was implemented in Virtex FPGA kit.

Index terms--Binary to Excess-1 Converter (BEC), Carry Select Adder (CSLA), Linear CSLA, Vedic Multiplier (VM), UrdhvaTiryakbhyam.

I.INTRODUCTION

The building block of a DSP processoris an adder circuit.Butdigital adder has a drawback of propagation delay. Bedrijisuggested [5] that the problem with carry propagation delay is solved by independently generating multiple radixes,carries and due to this carries for selection between simultaneously generated sums.AkhileshTyagi bought a scheme for generation of carry bits with block carryin 1 from the carries of a block with block carryin0 [11]. Chang and Hsiao made a proposal [4] that aCSLA scheme using BEC replacing one RCA.A multiplexer based add one circuit was forwarded by Youngioon Kim and Lee Sup Kimto for

, Gunakasamuchyah, Gunitasamuchyah, NikhilamNavatashcaramamdashatahreducing the area. Ramkumar and Harish made a proposal of [2] Binary to Excess-1 Converter (BEC) technique, an efficient and easier gate level modification to resize by reducing the area of linear CSLA.

CSLA is widely employed to rectify the issues of carry propagation delay through the generation of multiple carries and then selecting a carry for the generation of the sum [5]. It uses multiple pairs of RCA for the generation of partial sum and carry by considering carryin0 and carryin 1, then the final sum and final carry gets selected by the multiplexers (Mux). The ground idea of the above said work is using BEC instead of RCA with carryin 1 in Regular CSLA for achieving less area [7], [4] and [1]. The top benefit of BEC is from the reduced number of logic gates compared to the nbitFull Adder (FA).

The word usage ―Vedic is taken from the word ―Veda which refers to the store-house of knowledge. Vedic Multiplier (VM) architecture differs by lot of means from the Conventional technique of multiplication such as add and shift [12]. Vedic Multiplier has its grounds on ancient Indian Vedic Mathematics. Vedic mathematics is basically upon 16 Sutras (formulae) like Anurupyeshunyamamyat, Chalana-kalanabhyam, EkadhikinaPurvena,EkanyunenaPurvena, Paraavartyayojavet, Puranapuranabhyam, sankalanavyavakalanabhyam,Shesanyankenachara mena,Shunyamsaamyasamuccaye,Sopaantyadvaya maantyam,UrdhvaTiryakbhyam, Vyashtisamanstih and yaavadunamthat deals with various branches of mathematics like arithmetic, algebra, geometry etc [10]. Vedic Multiplier (VM) is reliable and an efficient one compared with Array Multiplier and Booth Multiplier based on area and speed [9].

Section II is regarding the details of BEC. The area evaluation methodology of modified linear CSLA is portrayed in section III. The next section is regarding Vedic Multiplier that uses CSLA's.

II. Binary to Excess 1 converter

The ground idea regarding this work is using BEC instead of RCA with carryin 1 to reduce the area of the Regular Linear CSLA as well as Regular linear CSLA. For replacing the n-bit RCA, an n+1-bit BEC is required. General structure and the basic function of 3-bit BEC are shown in Fig 1 and Table

1, respectively.Boolean expressions for 3-bit BEC is as given below (functional symbols: & AND, ~ NOT, ^ XOR).

Table 1. Function of 3-bit BEC

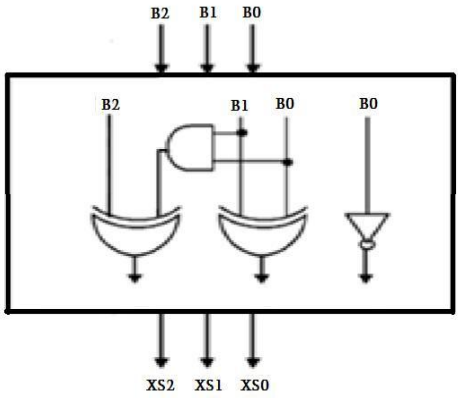
B [2 : 0]			X S [2 : 0]		
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

XS0=~B0

XS1=B0^B1

XS2=B2^(B0&B1)

Fig 1. 3-bit Binary to Excess 1 Converter



III. AREA EVALUATION TECHNIQUE OF 16-BIT MODIFIED LINEAR CSLA

The general structure of the 16-bit Modified linear CSLA is as depicted in Fig 2. It is with 5 groups of different size of BEC and RCA. Each group contains an RCA, one BEC and one Multiplexer. In the Modified linear CSLA, the group2 comprises of one 2-bit RCA which has 1 FA and 1 HA for carryin 0. Instead of another 2-bit RCA with carryin 1, a 3-bit BEC is used that adds one with the output of 2-bit RCA.6:3 Mux's selection input is c3. When c3 = 0, the multiplexer selects RCA output orelse BEC output gets selected. The group2's output are Sum [3:2] and carryout, c3 and then area count of group2 can be determined as follows:

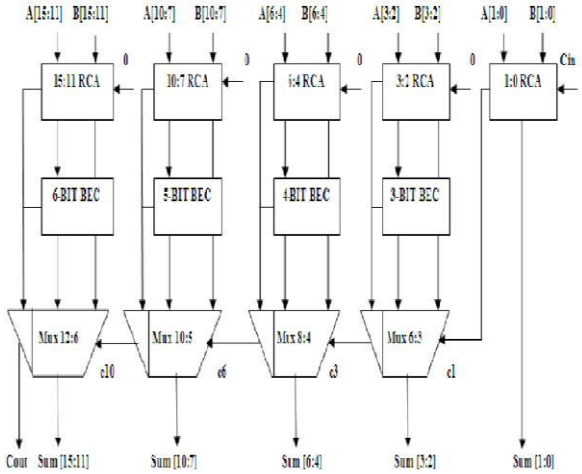
Gate count=43(FA + HA + Mux + BEC)
FA = 13 (1*13) HA = 6
(1 * 6) Mux = 12 (3 * 4) NOT = 1 AND = 1 XOR = 10 (2 * 5) BEC (3-BIT) = NOT + AND + XOR = 12

Similarly the estimated area of the other groups in the Modified linear CSLA are evaluated and listed in Table 2.

Table 2. Area count of 16 bit Modified Linear CSLA

GROUP	AREA COUNT
Group1	52
Group2	89
Group3	89
Group4	89

Fig 2. 16 Bit Modified Linear CSLA



IV. VEDIC MULTIPLIER

In this discussion the Vedic Multiplier(VM) is mainly based on UrdhvaTiryakbhyam (multiplication sutra) of ancient Indian Vedic Mathematics. UrdhvTiryakbhyamgenerally means Vertical and crosswise respectively. This strikes the contrary in the actual multiplication process itself. This formula help proceeding parallel generation of partial products and eliminates unwanted multiplication process steps. Vedic Multiplier has a merit that as the number of bits increases, area and gate delay also increases too slowly compared to other multipliers. Therefore it is the time, power and area that are efficient. In Fig 3, the digits on the either side of the line are multiplied and added by the carry of the preceding step. It does generate a carry and one of the bits of the results. This carry is to be added with the next step multiplication result and so the process goes on moving. If more than

one line is seen in one step, all obtained results are then added to the carry of previous step. In each step bit and all other bits act as carry for the next step and the least significant bit (LSB) acts as the result. The multiplication of two 4X4 bit and 2X2 bit binary numbers are as depicted in Fig 3 and Fig 4 respectively.

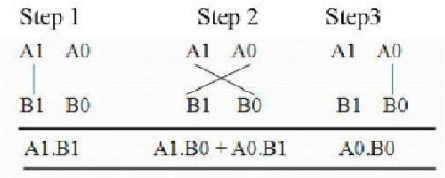


Fig 3: 2X2 bit binary multiplication using Urdhva Tiryakbhyam

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S0 = A0B0
C1S1 = A1B0 + A0B1
C2S2 = C1 + A1B1
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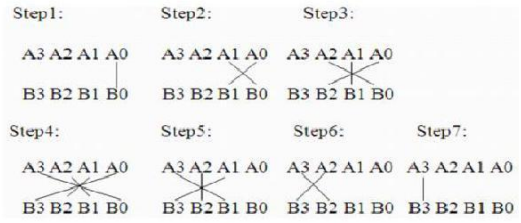

Fig 4: 4X4 bit binary multiplication using Urdhva Tiryakbhyam

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S0 = A0B0
C1S1 = A1B0 + A0B1
C2S2 = C1 + A1B1 + A2B0 + A0B2
C3S3 = C2 + A3B0 + A0B3 + A1B2 + A2B1
C4S4 = C3 + A3B1 + A1B3 + A2B2
C5S5 = C4 + A3B2 + A2B3
C6S6 = C5 + A3B3
Final result: C6S6S5S4S3S2S1S0
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VM is of three stages.The 1st stage consists of Multiplication unit, 2nd stage isof partial products and carry and the 3rd stage: adder and the result of multiplication. In the third stage adder block, CSLA can be used.

A. Basic block of Vedic Multiplier

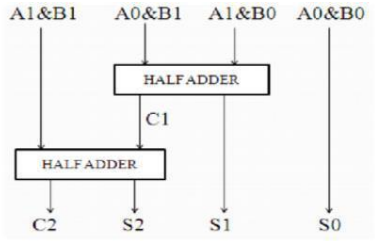

Fig 5: fundamental block of VM

In Vedic multiplier design, a 2X2 bit block is one ofthe fundamental block is shown in Fig 5. Also this same fundamental block is taken as a Multiplication unit block of

4X4 bit Vedic Multiplier.Considering the two 2-bit binary numbers A1A0 and B1B0. The obtained result of this 2X2 bit multiplication would be found as 4 bits that is C2, S2, S1 and S0. The least significant bit(LSB)A0 of the multiplicand is vertically multiplied with least significant bit(LSB) B0 of the multiplier,To obtain their product S0 and this S0 is the least significant part of obtained result (S0). Then A1 and B0, and A0 and B1 are multiplied incross, add the two, get sum1 (S1) and carry1 (C1), the sum bit can be said as the middle part of the result (S1). Then A1 and B1 is multiplied in vertical, and is added with the previous carry (C1) and get S2 as their product and carry2 (C2), the sum bit will be down to the result (S2). Then the carry2 (C2) is considered as the most significant part of the result (S3).

B. 4x4 bit Vedic Multiplier

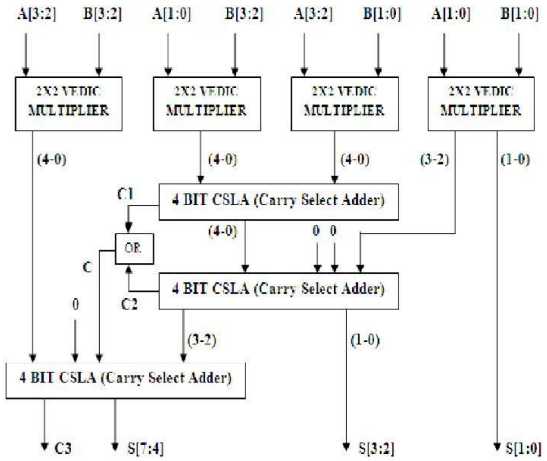

Fig 6: Block diagram of 4x4 Vedic multiplier

The design of 4X4 bit Vedic Multiplieris shown in Fig 6. In this design, the 1st stage is of 2X2 bit block (fundamental block) as a Multiplication unit. The 2nd stage comprises of carry and partial products. Then the 3rd stage comprises of 4 bit CSLA (4 bit Regular Linear CSLA , 4 bit

Modified Linear CSLA, 4 bit Regular linear CSLA and 4 bit Modified linear CSLA) and 8 bit result of multiplication. The initial step in the design of 4X4 bit VM is grouping the 2 bit of each 4 bit input. These pairs constitute vertical and crosswise product terms.A separate 2X2 bit VM block does the handling ofeach input bit.The schematic of a 4X4 bit block is designed using 2X2 bit blocks. The partial products represent the Urdhva vertical and cross product terms.

C. 8x8 bit Vedic Multiplier

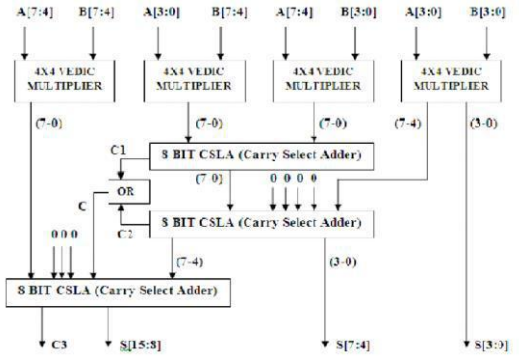

Fig 7: Block diagram of 8x8 bit Vedic Multiplier

The design of 8X8 bit VM is drawn in Fig 7. Here the first stage consists of 4X4 bit block as a Multiplication unit. The second stage is of carry and partial. Then the third stage comprises of 8 bit Modified linear CSLA and 16 bit result of multiplication. The primary and initial step in designing of 8X8 bit block VM is to group the 4 bit of each 8 bit input. This pair forms the incross and vertical product terms.4X4 bit VM block handles each input bit pairs.The schematic depiction of 8X8 bit VM can be designed by 4X4 bit VM blocks.

D. 16x16 bit Vedic Multiplier

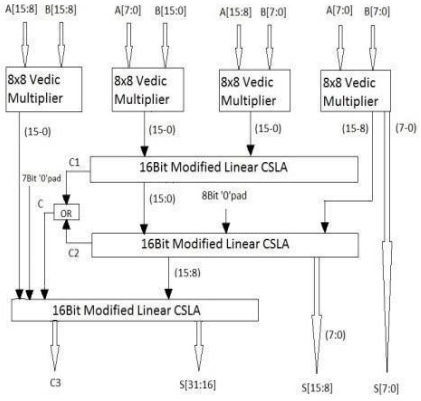

Fig 8: Block diagram of 16x16 bit Vedic Multiplier

The 16X16 bit VM's design drawn is in Fig 8. This design consists of first stage 8X8bit VM blocks,as a Multiplication unit. The second stage is of partial products and carry. Then the third stage is of 16 bit Modified linear CSLA and 32 bit result of multiplication. The initial step in designing of 16X16 bit VM is to group the 8 bit of each and every 16 bit input. The above said pairs forms incross and vertical product terms. Each input bit pairs are handled by a separate 8X8 VM block. The schematic depiction of a16X16 bit VM block can be designed using 8X8 bit VM blocks.

E. 32x32 bit Vedic Multiplier

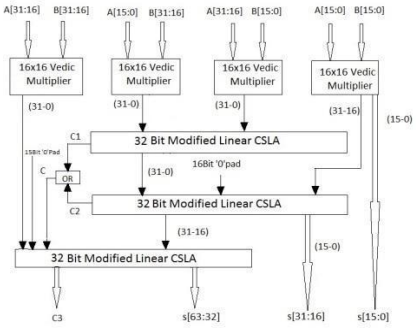

Fig 9:Block diagram of 32x32 bit Vedic Multiplier

Designing of 32X32 bit VM is as shown in Fig 9.Here the first stage is of 16X16 bit VM blocks as a Multiplication unit. The second stage comprises of carry and partial products. Then the third stage is of 32 bit Modified linear CSLA and 64 bit result of multiplication. The primary and initial step in the design of 32X32 bit VM is grouping the 16 bit of each 32 bit input. These pairs forms vertical, crosswise product terms. Separate 16X16 bit VM block handles each input bit pairs. The schematic depiction of 32X32 bitVM block can be designed using 16X16 bit VM blocks.

F. 64x64 bit vedic Multiplier

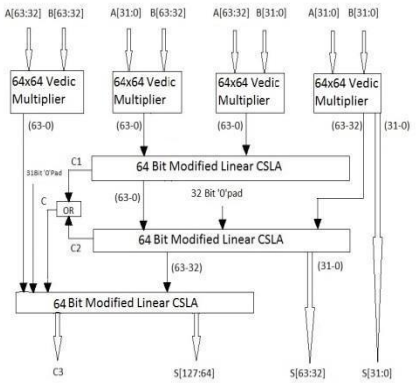

Fig 10: Block diagram of 64x64 bit Vedic Multiplier

Designing of 64X64 bit VM drawn in Fig 10.Here the first stage is of 32X32 bit VM blocks as a Multiplication unit. The second stage is of carry and partial products. Then the third stage comprises of 64 bit Modified linear CSLA and 128 bit resultsof multiplication. The primary and initial step in designing of 64X64 bit VM block is to group the 32 bit of each 64 bit input. These pairs forms vertical incross and vertical product terms.Separate 32X32 bit VM block handles each input bit pairs. The schematic depiction of a 64X64 bit VM can be designed using 32X32 bit VM blocks.

G. 128x128 bit Vedic Multiplier

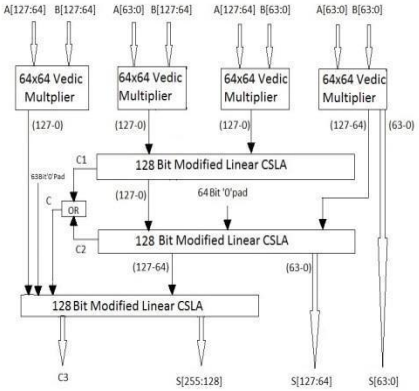

Fig 11: Block diagram of 128x128 bit Vedic Multiplier

Designing of 128X128 bit VM drawn in Fig 11.Here the 1st stage is of 64X64 bit VM blocks, as a Multiplication unit. The second stage is of carry and partial products. Then the third stage is of 128 bit Modified Linear CSLA and 256 bit result of multiplication. The primary and initial step in designing of 128X128 bit VM isto group the 64 bit of each 128 bit input. These pair forms incross and vertical product terms.Separate 64X64 bit VM block handles each and every input terms. The schematic depiction of 128X128 bit VM block can be designed using 64X64 bit VM blocks.

V. POWER REPORT

On-Chip	Power (W)	Used	Available
Logic	0.000	1705	66560
Signals	0.000	1938	---
IOs	0.000	508	633
Leakage	0.338		
Total	0.338		

VI. CONCLUSION

This paper comprises of simple technique that reduces the area and delay of CSLA architectures that are used in Vedic Multipliers. The advantage of using reduced number of gates is that the area gets reduced and the result analysis proves to be effective comparing with other multipliers that use various other techniques. Therefore the Modified Linear Carry Select Adder is indeed an effective architecture that is simple and area efficient for VLSI hardware implementation.

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