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An Efficient VLSI Implementation for 128bit Modified Linear CSLA

G. Praveen kumar [1] ,V.Pradeep[2], P.Karthikeyan[3],K.Akshay[4]
B.E Electronics and Communication Engineering, S.N.S college of technology.

Abstract: The carry select adder is one of the fastest adder. The area, propagation delay and power consumption of regular linear CSLA is very high. To improve the performance of this adder, the architecture design of regular linear CSLA has to be modified. In the modified linear CSLA, the implementation of binary to excess converter paved way for low power consumption and also reduces propagation delay. This design can be utilized in many areas like signal processing, integrated circuit designs, etc... The result analysis of this paper shows that modified linear CSLA has better advantages compared to regular linear CSLA.

Index terms: ***Carry select adder (CSLA), ripple carry adder(RCA),binary to excess converter and multiplexer(MUX).***

I. INTRODUCTION

VLSI is one of the recent developing trends that is used to implement any process involved in microprocessor, CPU and also in digital and analog devices just by using combinational circuits. By using this architecture, power efficiency and the propagation delay of any system can be determined.Binary adder is a combinational circuit that is used to perform the arithmetic addition of binary numbers. These adders play a vital role in electronics applications and in signal processing techniques. Among the adders, carry select adder has an upper hand of performing operations at high speed and accuracy. Propagation delay can be reduced by using the carry select adder (i.e.,) time taken by the system to respond to the given input. More emphasis has been laid upon modified linear CSLA. Modified linear CSLA can be designed for various range of bits. Here, the 128 x 128 (bit) modified linear CSLA has been designed by the means of verilog coding.

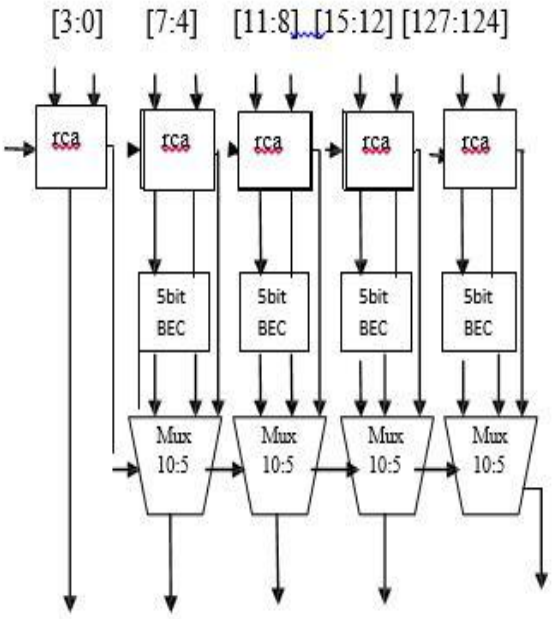


Fig1: Block Diagram of modified 16bit linear Carry Select adder

II. CARRY SELECT ADDER:

The carry select adder has many classifications like regular CSLA, modified square root CSLA ,modified linear CSLA, etc.,,. CSLA generally works as a selection of carry from the addition of binary numbers. CSLA is actually power efficient and area efficient. But the speed becomes low because each full adder starts its operation only after the previous carry signal is ready. Generally, a ripple carry adder is a circuit which can perform addition operation by giving out both sum and carry. This modified linear CSLA has 3 blocks namely RCA , BEC and MUX .Each block does
different operations. For example, RCA does the addition operation which delivers the carry separately.

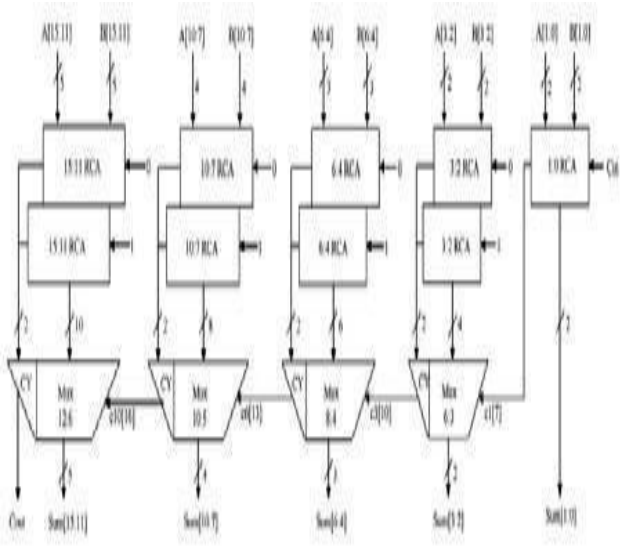


Fig 2: Block Diagram of Regular 16 bit Carry Select adder

The use of BEC in the CSLA resulted in better area efficiency . On the other hand, it is also utilised to reduce the propagation delay that occurs in the conventional CSLA. In the 16 bit modified linear CSLA , BEC has been used to obtain better power efficiency. The ripple carry adder generally consists of full adders. In this design, a 4 bit ripple carry adder containing four full adders is used. Full adder does the general operation of adding the binary numbers and giving out the carry along with the sum

A full adder has 2 inputs and an output .An additional input is given to indicate that the adder is in high or low state.

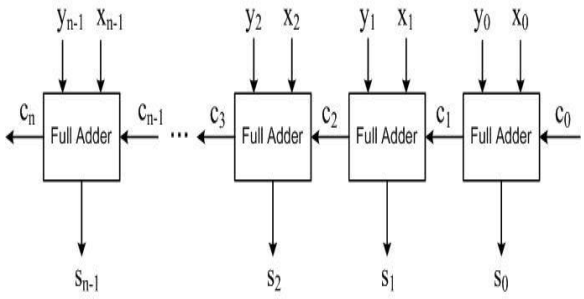


Fig 3: Ripple carry adder architecture for n bit

BEC is a simple process of adding 011 to the binary output from the RCA. As mentioned above, the CSLA contains BEC, which is a 5 bit component . 5 inputs are given to it and 5 outputs are taken out from it. It also delivers a carry separately along the output. The main advantage is that it eliminates the propagation delay which generally occurs in the regular CSLA. The main composition of BEC is only AND(&),NOT(~)and XOR(^). The first XOR gate , is being given 2 inputs directlyand for the 2nd XOR gate, input is given bydoing AND operation for the inputs of 1st XOR gate and the other input is given directly. Likewise, the connection is done for the rest of the bits .On the other hand, the1st output alone is achieved by the inversionoperation using NOT gate operation.

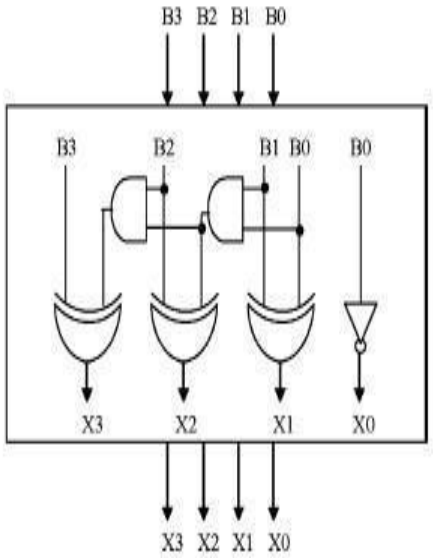


Fig 4: Circuit diagram for BEC

MUX generally means **many to one function**. Multiplexer has „ n" number of inputs , „m" number of control signals and an output. In this CSLA , the 10:5 MUX is used, which means 10 inputs and 5 outputs along with a selection line to select the required input . The carry from each block of RCA and BEC is sent as an input to the MUX. The MUX also sends the carry, which is used as a selection line for the next MUX and the final carry is taken as a separate output .As there are 15 inputs we will obtain the same number of outputs. Along with the resultant outputs, carry output (cout) is also obtained.

III. ANALYSIS OF OTHER ADDERS:

A.Carry Skip Adder:

The general operation of carry skip adder is that it divides the total number of words into „ k" number of bits and does its operation. Due to the division of words into a number of different bits, it consumes some time to perform its operation and so, it is not fast and area efficient. But, the modified linear CSLA overcomes all these disadvantages witnessed in the carry skip adder. Hence, this CSLA is used in many areas for the process of addition. Even a 32 or 64 or any number of bit operation can be performed using CSLA. The skip adder also has a disadvantage that it skips some stages while it is in process and leads to some error in the obtained output.

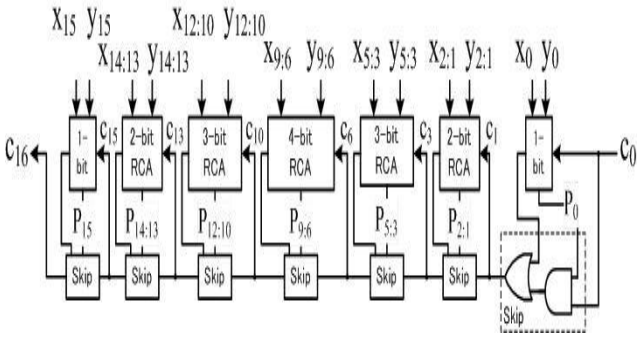


Fig 5:Block Diagram of Regular 16bit Carry skip adder

B. Carry Save Adder:

The carry save adder is used wherever there is a necessity of adding n- number of bits . It works in straight forward Hmanner (i.e) it adds the first two numbers and then add that sum to the next and so on.The carry save adder is also a type of a digital adder which also gives out the sum and the carry . Through this adder, we can also achieve the desired result easily but its area efficiency is not upto the mark when compared with the modified linear CSLA. It differs from other digital adders, by the fact that the output obtained would be of the same dimension of the input. This is considered as one of the advantages of the carry save adder.

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	50	66,560	1%
Number of occupied Slices	28	33,280	1%
Number of Slices containing only related logic	28	28	100%
Number of Slices containing unrelated logic	0	28	0%
Total Number of 4 input LUTs	50	66,560	1%
Number of bonded IOBs	51	633	8%
Average Fanout of Non-Clock Nets	2.17		

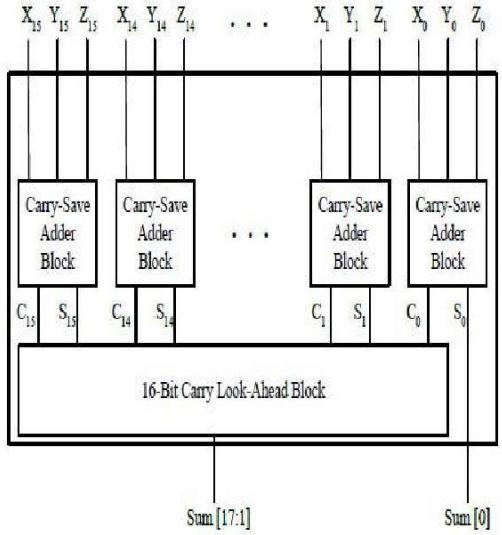


Fig 6: Block Diagram of Regular 16bit Carry Save adder

IV.DELAY ANALYSIS

In this design, some of the RCA blocks are replaced with the BEC, that leads to reduced area and propagation delay .The propagation delay and area count of the modified linear CSLA for a range of bits are compared and analysed. The results are clearly demonstrated with a neat chart.

Table1: gates for BEC

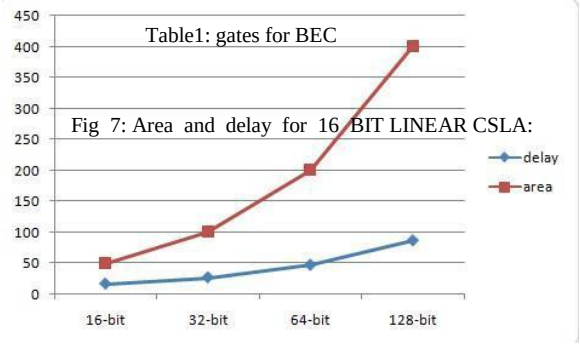


Fig 7: Area and delay for 16 BIT LINEAR CSLA:

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	100	66,560	1%
Number of occupied Slices	55	33,280	1%
Number of Slices containing only related logic	55	55	100%
Number of Slices containing unrelated logic	0	55	0%
Total Number of 4 input LUTs	100	66,560	1%
Number of bonded IOBs	99	633	15%
Average Fanout of Non-Clock Nets	2.19		

Maximum combinational path delay: 26.685ns

Fig 8: Area and delay for 32 BIT LINEAR CSLA

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	200	66,560	1%

Maximum combinational path delay: 46.867ns

Fig 9: Area and delay for 64 BIT LINEAR CSLA

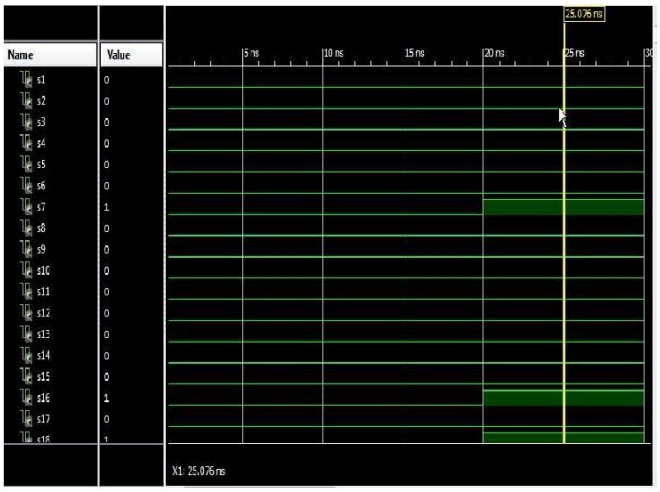
Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	400	66,560	1%
Number of occupied Slices	220	33,280	1%
Number of Slices containing only related logic	220	220	100%
Number of Slices containing unrelated logic	0	220	0%
Total Number of 4 input LUTs	400	66,560	1%
Number of bonded IOBs	387	633	61%
Average Fanout of Non-Clock Nets	2.21		

Maximum combinational path delay: 86.254ns

Fig 10: Area and delay for 128 BIT LINEAR CSLA:

V.SIMULATION RESULTS:

The simulation results for the above specified 128-bit modified linear CSLA has been depicted clearly using Xilinx software.



VI.CONCLUSION

In this paper, 128-bit modified linear CSLA has been designed using the verilog codings. The power of carry select adders gives a clear idea that it has high performance characteristics and less complexity when compared with the carry save and carry skip adders. It can be concluded that modified regular linear CSLA is superior with its

unique features. The novelty of our approach is been justified by the calculated comparison made with that of the results obtained by Xilinx simulations.

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Authors Profile

G.Praveen kumar pursuing B.E in Electronics and Communication Engineering at S.N.S college of technology. His areas of interest are VLSI design, PIC microcontroller and Arduino programming.

V.**Pradeep** pursuing B.E in Electronics and Communication Engineering at S.N.S college of technology. His areas of interest are VLSI design, PIC microcontroller and Automation.

P. Karthikeyan pursuing B.E in Electronics and Communication Engineering at S.N.S college of technology. His areas of interest are VLSI design, Automation and PLC.

K.Akshay pursuing B.E in Electronics and Communication Engineering at S.N.S college of technology. His areas of interest are VLSI design and PIC microcontroller programming.