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A Review Paper On Generalization and Parameter Variation of Different PLL structures

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***Abstract*—A Phase locked loop(PLL) is a closed loop feedback control systemwhich interlocks both the phase and frequency of the output signal with the input signal.PLL typically consists of three parts .they are: Phase Detector (PD), low pass filter or loop filter (LP) and voltage control oscillator(VCO).In the design of the PLLs integrator ,proportional-integrators are incorporated. Depending on the number of poles at the origin of the design the PLLs are classified into TYPE I, TYPE-II and TYPE-III etc. Different PLLs are designed to achieve fast dynamic responses, high filtering capabilities, stability and effective response behavior. In this paper we propose the generalized method to classify the PLL based on the presence of the poles at the origin. Different parameters are analyzed for all the three types of PLLs.**

Index terms -Phase locked loop (PLL), phase detector (PD), loop filter (LP), voltage controlled oscillator (VCO).

I. INTRODUCTION

The phase locked loop (PLL) found wide usage in the field of communication for the synchronization of the communication systems[1-3]. PLL is the core component for the purpose of the phase locking. PLL is the feedback control system which interlocks or synchronizes the phase and frequency of the output signal with input signal. PLL is made up of three parts: phase detector (PD), Low pass filter (LP). The basic topology of the conventional simple PLL is shown in the Fig.1

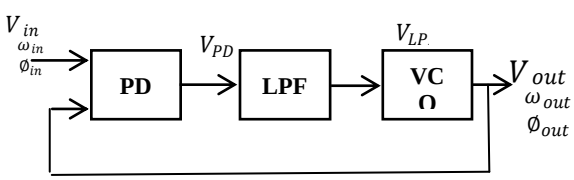

Fig.1 Simple PLL structure

$$V_{in}(t) = V_A cos\omega_1 t \quad (1)$$
$$V_{out}(t) = V_B \cos(\omega_1 t + \phi_0) \quad (2)$$

PD is a basic block of the design which produces voltage V_{PD} and the high frequency component for the corresponding phase difference between the input signal and the feedback signal. The undesired high frequency of the output is filtered out by using the loop filter (LP) which is the low pass filter(LPF). Thus the filtered output is fed to the input of the oscillator which is VCO which produces the corresponding phase and frequency of the desired signal.The feedback loop compares the phases of the input and the output signals and doesn't require the knowledge of the voltage or the currents in their feedback operation thus giving a wider area for the design of the PLLs. For example, the PLL can be designed with the help of Operational Trans resistance Amplifier(OTRA) [4].

While designing the PLL we assume the Linear, Continuous-time model and validity of results of PLL pertain to the limited operating frequencies.In the aspect of the PLL design we incorporate integrators, Proportional, Proportional-integrator in the PD and VCO as well and also zeros at the origin depending upon the stability condition. From these controllers we determine the Type and Order of the PLL designed. The Type of the PLL is determined from the number of poles present at the origin in the loop forward path. In designing a PLL parameters considered are bandwidth, the desired high frequency roll-off, transient behavior and also the stability of the PLL. The loop filter can be of any order. There are many tradeoffs between the parameters in the PLL designing. These are compensated by introducing the resistors and capacitors in the forward path and by varying the electrical values of the components.

II. DYNAMICS OF SIMPLE TYPE I PLL

The conventional simple linear model of the TYPE I PLL model is presented in the Fig.2

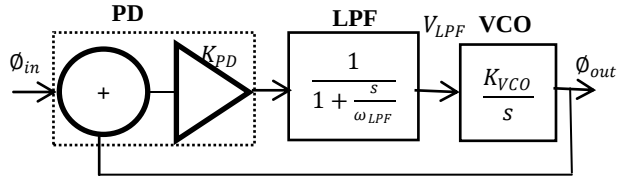

Fig.2 TYPE I PLL Model

The open loop transfer function of the conventional PLL is given by the equation

$$G(s) = \frac{K_{PD}\,K_{VCO}}{s}\,LP(s) \quad (3)$$

Where K_{PD} denotes the gain of the PD, LP(s) denotes the loop filter transfer function and the VCO is modeled by the Integrator. Sincethe presence of the single pole at the origin it is TYPE I PLL. The closed loop transfer function is given by

$$H(s) = \frac{G(s)}{1+G(s)} = \frac{K_{PD}\,K_{VCO}}{\frac{s^2}{w_{LPF}} + s + K_{PD}\,K_{VCO}} \quad (4)$$

Comparing thetransfer function with the second order transfer function where $\zeta$is the "damping ratio" and ω_n is the "natural frequency". The second order transfer is given by

$$H(s) = \frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \quad (5)$$

$$\text{Where } \omega_n = \sqrt{w_{LPF} K_{PD} K_{VCO}} \quad (6)$$

$$\zeta = \frac{1}{2}\sqrt{\frac{w_{LPF}}{K_{PD} K_{VCO}}} \quad (7)$$

$$\zeta\omega_n = \frac{1}{2} w_{LPF} \quad (8)$$

The transfer function in the (4) can be generalized and denoted as

$$H_I(s) = \frac{H_N}{H_D(s)} \quad (9)$$

Where $H_N$are a constant and independent of $H_D(s)$ and the DC gain of the system is unity. The high frequency roll- off factor for the noise transfer function can be obtained from the order of the denominator.

TYPE I PLL suffers from the trade-off between the settling speed, the ripple on the control voltage(i.e. the quality of the output signal), the phase error and the stability of the system. The Type I PLL also suffers from another critical drawback: limited acquisition range of frequency.

III. DYNAMICS OF TYPE II PLL

To overcome the problems in the previous section mentioned Aided acquisition method is incorporated in the PLL design. In this design both frequency detector and charge pump are added to the conventional TYPE I PLL. The linear model of the simple charge-pump PLL is depicted in fig.3

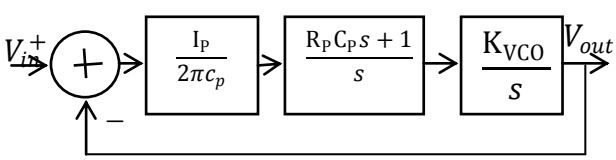

Fig.3 TYPE II charge pump PLL.

The open loop transfer function is given by

$$G(s) = \frac{I_P}{2\pi}\left(R_P + \frac{1}{C_P S}\right)\frac{K_{VCO}}{S} \quad (10)$$

Since two poles at the origin it is TYPE II PLL. The closed loop transfer function H(s) is

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P S+1)}{S^2+\frac{I_P}{2\pi}K_{VCO} R_P S+\frac{I_P}{2\pi C_P}K_{VCO}} \quad (11)$$

$$\text{Where } \omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P}} \quad (12)$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi}} \quad (13)$$

The TYPE II PLL transfer function can be generalized to the form

$$H_{II}(s) = \frac{\omega_1 H_N + sH_N}{\omega_1 H_N + sH_D(s)} \quad (14)$$

When $\omega_1$is kept small H_{II} can be approximated toH_I. In the same way if the poles at origin and zeros at $\omega_2$are added at the origin the new transfer function obtained is:

$$H_{III}(s) = \frac{\omega_1\omega_2 H_N + s(\omega_1+\omega_2)H_N + S^2 H_N}{\omega_1\omega_2 H_N + s(\omega_1+\omega_2)H_N + S^2 H_D(s)} \quad (15)$$

From the eq. (9),(14) &(15) we note the regularity in the transfer function of the PLL and the generalized tabular form for the TYPE and Order[4] is summarized below in the tables I to III .

TABLE I- Type N- Order N PLLs

TYPE/	I/1	II/2	III/3

ORDER			
G(s)	$\frac{K_{PD}}{s}$	$\frac{K_{PD}.\omega_1}{S^2}$(1+s/ ω_1)	$\frac{K_{PD}.\omega_1.\omega_2}{S^3}(1+s/\omega_1)(1+s/\omega_2)$
H(s)	$\frac{1}{1+{}^{S}/_{K_{PD}}}$	$\frac{K_{PD}.\omega_1+K_{PD}.S}{K_{PD}.\omega_1+K_{PD}.S+S^2}$	$\frac{K_{PD}\omega_1\omega_2+s(\omega_1+\omega_2)K_{PD}+S^2K_{PD}}{\omega_1\omega_2K_{PD}+s(\omega_1+\omega_2)K_{PD}+S^2K_{PD}+S^3}$
K/ω_n/ ζ	$K_{PD}/K_{PD}/\_$	$K_{PD}/\sqrt{K_{PD}\omega_1}/\frac{1}{2}\sqrt{\frac{K_{PD}}{\omega_1}}$	NA

TABLE II- TYPE N- Order N+1 PLLs

TYPE/ ORDER	I/2	II/3	III/4
G(s)	$\frac{K_{PD}}{s}\frac{1}{(1+s/\omega_p)}$	$\frac{K_{PD}.\omega_1}{S^2}\frac{(1+s/\omega_1)}{(1+s/\omega_p)}$	$\frac{K_{PD}.\omega_1.\omega_2(1+s/\omega_1)(1+s/\omega_2)}{S^3(1+s/\omega_p)}$
H(s)	$\frac{K_{PD}.\omega_p}{K_{PD}.\omega_p+\omega_p s+s^2}$	$\frac{K_{PD}\omega_1\omega_p+K_{PD}\omega_p S}{K_{PD}\omega_1\omega_p+K_{PD}\omega_p s+\omega_p s^2+s^3}$	$\frac{K_{PD}\omega_1\omega_2\omega_p+s(\omega_1+\omega_2)K_{PD}\omega_p+S^2K_{PD}\omega_p}{\omega_1\omega_2\omega_pK_{PD}+s(\omega_1+\omega_2)K_{PD}\omega_p+S^2K_{PD}\omega_p+\omega_pS^3}$
K/ω_n/ ζ	$K_{PD}/\sqrt{K_{PD}\omega_p}/\frac{1}{2}\sqrt{\frac{\omega_p}{K_{PD}}}$	NA	NA

TABLE III – TYPE N- Order N+2 PLLs

TYPE/ ORDER	I/3	II/4
G(s)	$\frac{K_{PD}}{s}\frac{1}{(1+s/\omega_p)(1+s/\omega_{p2})}$	$\frac{K_{PD}.\omega_1}{S^2}\frac{(1+s/\omega_1)}{(1+s/\omega_p)(1+s/\omega_{p2})}$
H(s)	$\frac{K_{PD}\omega_p\omega_{p2}}{K_{PD}\omega_p\omega_{p2}+\omega_p\omega_{p2}s+(\omega_p+\omega_{p2})s^2+s^3}$	$\frac{K_{PD}\omega_1\omega_p\omega_{p2}+K_{PD}\omega_p\omega_{p2}s}{\omega_1\omega_p\omega_{p2}K_{PD}+\omega_p\omega_{p2}K_{PD}s+S^2\omega_p\omega_{p2}+(\omega_p+\omega_{p2})S^3+s^4}$

TYPE/ORDER	III/5
G(s)	$\frac{K_{PD}.\omega_1.\omega_2(1+s/\omega_1)(1+s/\omega_2)}{S^3(1+s/\omega_p)(1+s/\omega_{p2})}$
H(s)	$\frac{K_{PD}\omega_1\omega_2\omega_p\omega_{p2}+s(\omega_1+\omega_2)K_{PD}\omega_p\omega_{p2}+S^2K_{PD}\omega_p\omega_{p2}}{\omega_1\omega_2\omega_p\omega_{p2}K_{PD}+s(\omega_1+\omega_2)K_{PD}\omega_p\omega_{p2}+S^2K_{PD}\omega_p\omega_{p2}+\omega_p\omega_{p2}S^3+(\omega_P+\omega_{P2})s^4+s^5}$

Inorder to achieve high loop gain and for enhancing the ω_{pm} to achieve higher phase margin in less settling time and to reduce the locking time as well different design schemes are applied and also new mechanism are introduced. One among them is the increasing the Type and Order of the PLLs.

Adaptive PLL is one of the approaches to offer fast and smooth tracking of the phase-angle jumps [4]. In this method the gain of the frequency estimation loop is adjusted according to the input signal in-order to reduce the false frequency lock of the loop and phase angle jumps and initial startup stage of the PLL. Due to this approach undesired frequency transients and the phase oscillations are reduced drastically and the high speed in the phase angle estimation is obtained. Different parameters are taken into consideration for the different Types of PLL [6] and are summarized in the Table IV.

TABLE IV: Performance parameters of TYPE I, II and III PLLs.

PLL TYPES	TYPE -1	TYPE-2	TYPE-3
Phase Margin	66°	70°	85°
ω_{PM}(Mrad/S)	0.004	11.5	108
Rise Time	5 ms	120 ns	18 ns
Settling Time	5 ms	775 ns	215 ns
Overshoot	4.3	17.4	5.9
Damping ratio(ζ)	0.71	0.7	0.9

From the above table it is evident that gain loop, ω_{PM} increases; rise time and settling time or locking time decreases with the TYPE of the PLL. We can also draw the conclusion on the frequency,phase shift resolution and power consumption of the same TYPE II PLL in the different process technology.The tabular data depicts that frequency of operation, phase shift resolution increases with the decrease in the process technology length and the Power consumption decreases with the process technology [7]. The parameters are mentioned in the table V.

TABLE V: Variation of Performance parameters of the TYPE-II PLL withinprocess technology variation.

IV. CONCLUSION

Inthis paper the generalized notation form of the TYPEand Order of the PLL is proposed and thedependencies of the performance parameters acrossthe different TYPE and Order of the PLLs and also within the same TYPE II PLL with the variation ofthe process technology are examined. Type III PLL offers the high loop gain with the less locking time which drastically improved with Type of PLL. The power consumption also reduced with process technology variation within the same Type PLL.

Process	65nm CMOS	0.25 um CMOS	0.18um CMOS	MEMS	MEMS
Frequency	5.7 GH_Z	5 GH_Z	4 GH_Z	1-2 GH_Z	1GH_Z - 40GHz
Phase shift resolution	2.2°	10°	NA	5.6°	22.5°
Power consumption	10mW	60mW	65mW	NA	NA
Modulation	PSK	64-QAM	OOK	NA	NA

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