A Novel High-speed Two-operand Multiplier using CNFET Technology

Niloofar Charmchi
Faculty of Computer Engineering, University of Isfahan, Isfahan, Iran

MohammadReza Reshadinezhad
Faculty of Computer Engineering, University of Isfahan, Isfahan, Iran

***Abstract*-Multiplication is a crucial process in digital arithmetic, due to its application in multi-dimensional graphics, FIR filters, cryptography, etc. Researchers focus on reducing the power consumption and increasing the speed of multipliers. An approach to accomplish the desired goal is the use of nano-technologies in implementing circuits. Carbon nanotube technology is an appropriate option among emerging nano-devices, due to its similarities to the preceding technology, MOSFET. In this paper, an architectures for a four-bit two-operand multiplier is proposed. Theproposed multiplier and the previous four-bit two-operand multiplier are designed, implemented and simulated through carbon nanotube field effect transistors. Evaluations and comparisons are carried out through HSPICE simulator, using carbon nanotube technology. The simulation results indicate that the proposed four-bit two-operand carbon nanotube multiplier has a better performance in comparison to the preceding one.**

Keywords: Carbon nanotube field effect transistor, Fast multiplication, High speed multiplier, Nanotechnology, Wallace multiplier.

I. INTRODUCTION

Multiplication is an essential function in digital circuits and arithmetic units. Multi-dimensional graphics, digital filters and encryption methods employ multiplication in their functions [1]. This operation is time-consuming, due to adding a vast number of partial products to accomplish the final result. Therefore, reducing power and increasing the speed of this circuit is crucial for designers and manufacturers.Multiplication comprises three phases. First, each multiplicand bit multiply to a weighted bit of the multiplier. In this way, partial products are generated through bitwise AND. Second, partial products are reduced to two vectors of sum and carry, using compressors, Wallace and Dadda tree [2-4]. In the final stage, there is a carry propagating adder that computes the final multiplication result [2, 5].Some studies diminish partial products generation time through algorithms like Booth encoding, which cuts partial products to half [6, 7].A number of publications suggest methods for decreasing time of partial product reduction phase [8-10]. Eventually, some researches apply fast adders in the final stage of multiplication [2, 5].

According to Moore's law, the number of transistors on a chip doubles every 12-18 months; hence channel length should be diminished. This phenomenon is called scaling and causes several problems such as short channel effect, parameters variations, etc [11]. In order to cover the issue of scaling, new technologies like carbon nanotube field effect transistor (CNFET), single electron transistor (SET) and quantum-dot cellular automata (QCA) are emerged [12-15]. Carbon nanotube transistor is an appropriate alternative for MOSFET circuits among these nano-technologies.MOSFETs and CNFETs have similar electrical and physical features that cause carbon nanotube technology to be a proper choice for the next generation arithmetic circuits. Moreover, CNFETs become center of attention due to low delay and power consumption [11].

A high-speed two-operand multiplier is proposed in this paper, which utilizes CNFET technology for a better performance. The proposed multiplier enhances delay and PDP parameters in comparison to the preceding multiplier.

II. A REVIEW OF CARBON NANOTUBE FIELD EFFECT TRANSISTORS

Carbon nanotube is a sheet of graphene that rolls up and shapes the graphene into a tube. It is presented with a Chirality vector, $Ch=n\overrightarrow{a_1}+m\overrightarrow{a_2}$. The ($n$, m) are Chirality numbers and $[\overrightarrow{a_1},\overrightarrow{a_2}]$are unit vectors. According to n and m, carbon nanotubes are divided into three groups. If $n=m$, then nanotube is called armchair. If $n=0$ or $m=0$, nanotube is zigzag and otherwise, it is chiral [16]. Three types of carbon nanotubes are shown in Fig. 1.

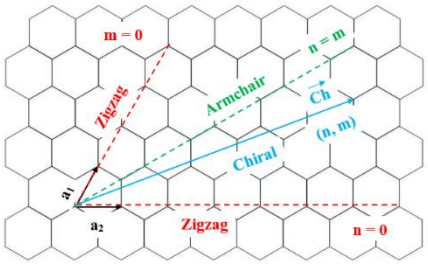


Figure 1. Sheet of graphene that forms three types of nanotubes

Armchair nanotubes have electrical features just like metals, whereas only one third of zigzag and chiral nanotubes have electrical properties and the rest act as semiconductors. If different voltages apply to a conductor carbon nanotube, an electrical current will be generated (like a wire). By applying a negative voltage to one side of the nanotube and a positive voltage to the other side, electrons flow in a direction leading to the positive pole. The electricity current in a carbon nanotube is conducted better than a metal. There is a resistance against electrons flowing in the metal, which is occurred in a collision with metal atoms. Conversely, electrons movement in a carbon nanotube is based on quantum mechanics, which leads to a wave-like flow and there is no collision in this case. Here, the quantum movement is called ballistic transport and it is a vital attribute for carbon nanotubes [17].

Furthermore, depending on the number of tubes, carbon nanotubes categorized in two groups of single-walled carbon nanotubes (SWCNT) and multi-walled carbon nanotubes (MWCNT) [14]. Each CNT has a diameter that can control the threshold voltage of a CNFET. This diameter is calculated as equation 1.

$$D_{CNT} = \frac{a}{\pi}\sqrt{n^2 + nm + m^2} = 0.0783\sqrt{n^2 + nm + m^2} \qquad (1)$$

Where, *a*is the carbon to carbon distance and computed via $a = \sqrt{3}a_0$ formula anda_0 = 0.142 *nm* is the length of the carbon-carbon bond. Moreover, *n* and *m* are chirality numbers.

The threshold voltage of a carbon nanotube transistor is controlled through adjusting the CNT diameter (equation 2).

$$V_{th} = \frac{\sqrt{3}}{3}\frac{av_{\pi}}{eD_{CNT}} \approx \frac{0.43}{D_{CNT}} \qquad (2)$$

Where, v_{π} is the π-π bond energy in the tight bonding model, equal to 3.033 *eV* and*e* is the unit electron charge. As it is shown in equation 2, the threshold voltage of a carbon nanotube field effect transistor is approximated as the inverse function of the nanotube diameter.

III. PREVIOUS WORKS

Multiplication is one of the essential operations in digital arithmetic. It is not a fast process, due to adding a large number of partial products and get the final result. Multiplication operations carry out in three stages. Most studies have focused on the second step of this operation, which is partial product reduction phase. In this section, previous two-operand multipliers are introduced.

There are several articles introduced various techniques of multiplier implementations. Callaway et al. presented four methods for implementing a two-operand multiplier and compared them in terms of power consumption, delay and PDP. Modified array, split array, Wallace tree and booth recoded Wallace tree were types of multipliers were investigated by Callaway et al. Authors proved that the fourth multiplier has the maximum power consumption and Wallace tree multiplier has the minimum PDP among other designs [18].

Itoh et al. presented a multiplier with rectangular-style Wallace tree. They were aiming to decrease chip size; hence, a reduction in layout cost and chip fabrication [9].

A low power Wallace multiplier based on wide counters was proposed by Abed et al. in 2011. This multiplier operated like Wallace multiplier, but there is a difference in the partial product reduction stage. In this stage, the proposed multiplier employed counters, instead of full adders; therefore, this circuit had fewer gates and also, consumed less power. This method showed its superiority in the case of carry propagation, because counters do not have input carry, while compressors have [19].

A four-bit two-operand CNFET-based multiplier was presented in [6], which utilizes low complexity Wallace tree for partial product reduction stage and also a ripple carry adder as the final carry propagating adder [20] (Fig. 2). This method employs less half adders for the reduction phase and the number of gates used in the circuit is decreased, consequently. However, this operation results in increasing the final carry propagating adder length; hence, a reduction in multiplier's speed.

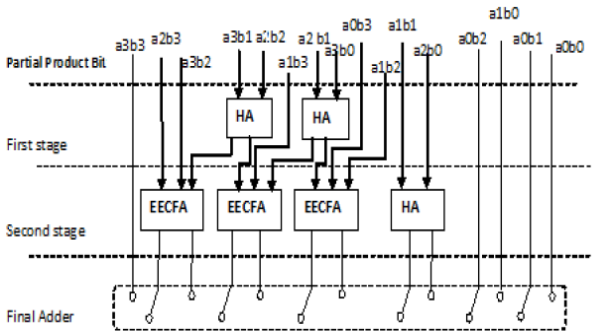


Figure 2. Low complexity Wallace multiplier architecture [6]

This multiplier utilizes an energy efficient carbon nanotube full adder based on XOR function, which reduces the power consumption of the circuit [21]. The nanotube architecture of this low complexity Wallace multiplier using CNFET-based AND, half adder, full adder and carry propagating adder is shown in Fig. 3.

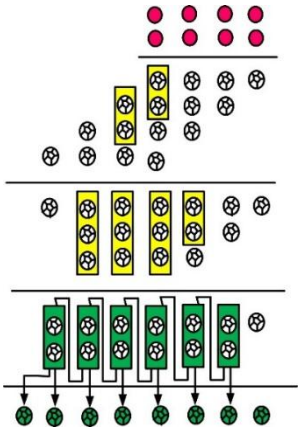


Figure 3. Low complexity Wallace multiplier presented in [6] based on carbon nanotube technology

This multiplication is carried out through three half adders, three full adders and a 6-bit carry propagating adder, which results in an eight bit output.

An implementation of a two-operand multiplier was introduced in [22], which was designed based on carbon nanotube technology.

IV. Proposed Four-bit Two-operand Multiplier

The proposed multiplier utilizes a high speed full adder illustrated in Fig. 4. The CNFET-based full adder is proposed by Charmchi et al. and makes use of XOR-XNOR and Majority functions to produce sum and carry [23].

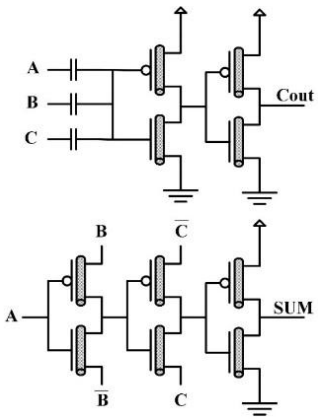


Figure 4. A CNFET-based full adder cell [23]

The proposed architecture for a four-bit two-operand CNFET-based multiplier, using nano-devices, is shown in Fig. 5.

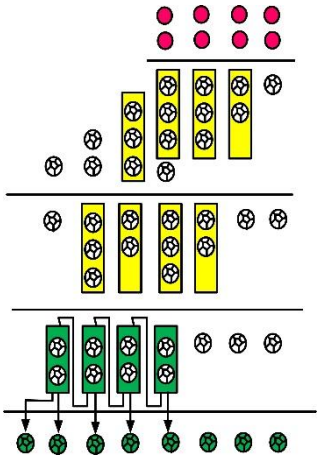


Figure 5. Proposed two-operand CNFET-based multiplier

The proposed multiplier utilizes eight full adders and a four-bit carry propagating adder, which leads to reduction in delay of the circuit,

V. Simulation Results

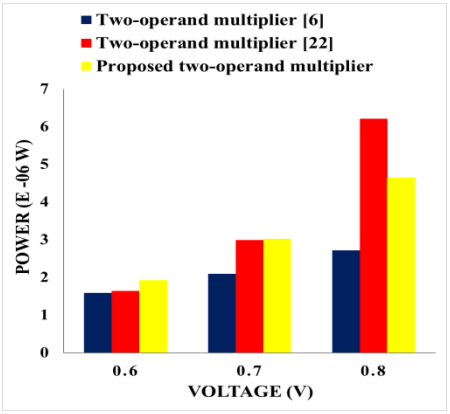
All simulations are performed on proposed two-operand multipliers, using HSPICE simulator andthe CNFET model [24-27] is utilizedin these simulations. This standard model has been designed for enhancement-mode unipolar MOSFET-like CNFETs, in which each transistor may include more than one carbon nanotube as its channel.

In order to show the superiority of the proposed design, power, delay and PDP is calculated for each implementation. PDP is a trade-off between power and delay of a circuit. Simulations are carried outin 0.6, 0.7 and 0.8 voltages and 3fF load capacitance. The results are tabulated in table 1.

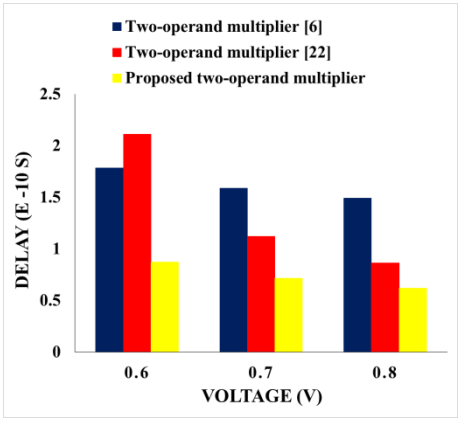
Table 1. Simulation results for multipliers at 3fF and 25$^{\circ C}$

	Power (e -06 W)	Delay (e -10 S)	PDP (e -16 J)
Multiplier	**0.6 v**		
Two-operand multiplier [6]	1.5813	1.785	2.8226
Two-operand multiplier [22]	1.6338	2.1114	3.4496
Proposed two-operand multiplier	1.9237	0.8733	1.6801
Multiplier	**0.7 v**		
Two-operand multiplier [6]	2.09	1.5888	3.3205
Two-operand multiplier [22]	2.9835	1.1234	3.3516
Proposed two-operand multiplier	3.0184	0.714	2.1554
Multiplier	**0.8 v**		
Two-operand multiplier [6]	2.7117	1.494	4.0512
Two-operand multiplier [22]	6.2085	0.865	5.3703
Proposed two-operand multiplier	4.638	0.6181	2.867

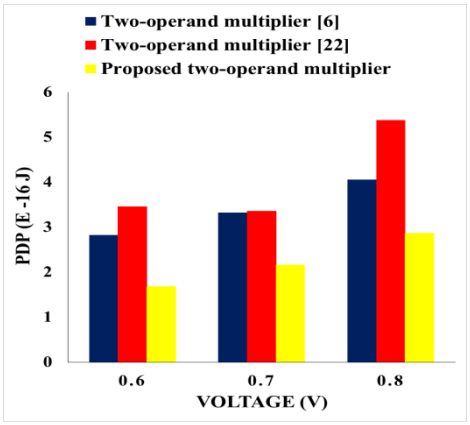
As it is shown in table 1, the proposed multiplier have better performance in delay and PDP parameters in comparison to the previous multipliers. What is more, the proposed design consumes more power in comparison with multiplier presented in [6], due to the number of full adders used in its architecture. The comparison of the preceding multipliers and the proposed two-operand multiplier isillustrated in Fig.6.



(a)



(b)



(c)

Figure 6. (a) Power, (b) delay, (c) PDP versus different voltages in multipliers

Simulation results at 0.6 V supply voltage and at 25^{oC} temperature with capacitance load of 3fF show that the proposed two-operand multiplier has 51% and 58% delay improvement in comparison to [6] and [22], respectively. The PDP improvement of proposed design at the same conditions is 40% and 51% with respect to the works of [6] and [22], respectively. At supply voltage of 0.7 V and at 25^{oC} temperature with capacitance load of 3fF, the results show 55% and 36% optimization in delay and 35% and 35.6% improvement in PDP parameter in comparison to multipliers presented in [6] and [22], respectively. Moreover, delay has 58% and 28% enhancement and PDP has 29% and 46% improvement in the case of 0.8v supply voltage, in comparison to [6] and [22], respectively.

The two-operand multiplier presented in [6] has less power consumption in comparison to the proposed design. This is due to the reduction of the number of gates in the design. On the other hand, the proposed two-operand multiplier has a full swing output that is an advantage for a digital circuit. Fig. 7 depicts the waveforms of the proposed design at 0.8 V supply voltage, 5fF load capacitance and 25^{oC} temperature.The design has well performed and has a full swing output in comparison to the multipliers of [6] and [22].

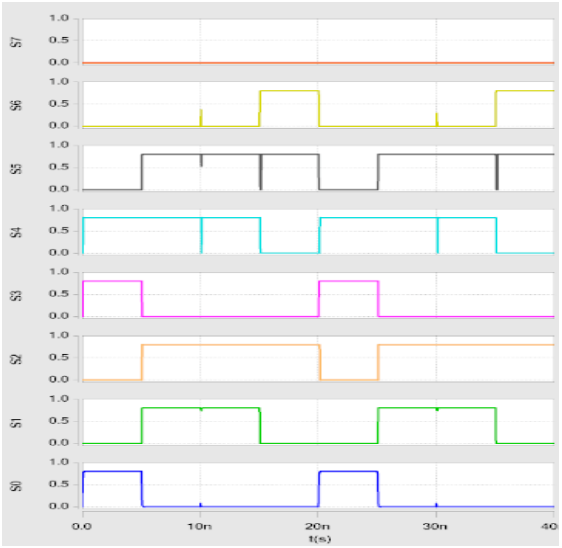


Figure 7. Output waveforms of the proposed two-operand multiplier

Accomplishing a high speed circuit is another benefit of the proposed method. The proposed multiplier has a better performance due to utilizing an XOR-XNOR and Majority full adder and a small carry propagating adder in the last step of the multiplication process.

VI. CONCLUSION

A high speed four-bit two-operand multiplier is designed and implemented in this article. The proposed design is based on carbon nanotube field effect transistor, which is the leading technology among nano-devices. The proposed multiplier utilizes small carry propagating adder in the final phase of the multiplication process; therefore, the delay of the circuit is reduced and the PDP parameter is improved. In contrast, the presented design consumes more power in comparison to the previous multipliers, due to adopting more full adders in its architecture in the reduction stage of multiplication.

REFERENCES

[1] Erdogan and T. Arslan, "Low power multiplication scheme for FIR filter implementation on single multiplier CMOS DSP processors," ElectronicsLetters, vol. 32, pp. 1959-1960, 1996.

[2] B. Parhami, Computer arithmetic: algorithms and hardware designs: Oxford University Press, Inc., 2009.

[3] C. S. Wallace, "A suggestion for a fast multiplier," IEEE Transactions on Electronic Computers, pp. 14-17, 1964.

[4] L. Dadda, "Some schemes for parallel multipliers," Alta frequenza, vol. 34, pp. 349-356, 1965.

[5] S .Murugeswari and S. K. Mohideen, "An Area Efficient and Low Power Multiplier Using Modified Carry Save Adder for Parallel Multipliers," in Mobile Communication and Power Engineering, ed: Springer, pp. 446-450, 2013.

[6] S. Mhaske, I. Ghosekar, and P. Bhaskar, "Low-Complexity Wallace Multiplier Using Energy-Efficient Full Adder Based On Carbon Nanotube Technology," International Journal of Engineering Research and General Science, 2015.

[7] R. McIlhenny and M. D. Ercegovac, "On the Implementation of a Three-operand Multiplier ",in Conference on Signals, Systems & Computers, pp. 1168-1172, 1997.

[8] J.-Y. Kang and J.-L. Gaudiot, "A fast and well-structured multiplier," in Euromicro Symposium on Digital System Design, 2004, pp. 508-515.

[9] N. Itoh, Y. Naemura, H. Makino, Y. Nakase, T. Yoshihara, and Y. Horiba, "A 600-MHz 54× 54-bit multiplier with rectangular-styled Wallace tree," IEEE Journal of Solid-State Circuits, vol. 36, pp. 249-257, 2001.

[10] N. Azimi, H. Hoseini, and A. Shahsavari, "Designing a Novel Ternary Multiplier Using CNTFET," International Journal of Modern Education and Computer Science, vol. 6, p. 45, 2014.

[11]G. Cho, Y.-B. Kim, F. Lombardi, and M. Choi, "Performance evaluation of CNFET-based logic gates," in Instrumentation and Measurement Technology Conference, IEEE, pp. 909-912, 2009.

[12]M. R. Reshadinezhad, M. H. Moaiyeri, and N. Kaivan, "An energy-efficient full adder cell using CNFET technology," IEICE transactions on electronics, vol. 95, pp. 744-751, 2012.

[13]K. Navi, H. H. Sajedi, R. F. Mirzaee, M. H. Moaiyeri, A. Jalali, and O. Kavehei, "High-speed full adder based on minority function and bridge style for nanoscale," Integration, the VLSI journal, vol. 44, pp. 155-162, 2011.

[14]Y. Maheswar, B. Raju, and K. S. Rajan, "Modelling and Characterization of CNTFET using Hspice," International Journal of Scientific & Engineering Research, vol. 4, 2011.

[15]M. R. Reshadinezhad and K. Navi, "High-speed multiplier design using multi-operand multipliers," International Journal of Computer Science and Network,2012.

[16] P. L. McEuen, M. S. Fuhrer, and H. Park, "Single walled carbon nanotube electronics," IEEE transactions on nanotechnology, vol. 1, pp. 78-85, 2002.

[17]R. D. Booker and E. Boysen, Nanotechnology for dummies: John Wiley & Sons, 2011.

[18]T. K. Callaway and E. E. Swartzlander Jr, "Power delay characteristics of CMOS multipliers," in 13th IEEE Symposium on Computer Arithmetic Proceedings, pp. 26-32, 1997.

[19]S. e. Abed, B. J. Mohd, Z. Al-bayati, and S. Alouneh, "Low power Wallace multiplier design based on wide counters," International Journal of Circuit Theory and Applications, vol. 40, pp. 1175-1185, 2012.

[20]R. S. Waters and E. E. Swartzlander Jr, "A reduced complexity wallace multiplier reduction," IEEE Transactions on Computers, vol. 59, pp. 1134-1137, 2010.

[21]M. Masoudi, M. Mazaheri, A. Rezaei, and K. Navi, "Designing high-speed, low-power full adder cells based on carbon nanotube technology," arXiv preprint arXiv:1411.2212, 2014.

[22]M. R. Reshadinezhad, N. Charmchi, and K. Navi, "Design and Implementation of a Three-operand Multiplier through Carbon Nanotube Technology," International Journal of Modern Education & Computer Science, vol. 7, 2015.

[23] N. Charmchi, M. R. Reshadinezhad and S. A. Ebrahimi, "A high-speed full Adder based on majority, XOR, XNOR functions through CNFET technology," unpublished.

[24]J. Deng and H. P. Wong, "A circuit-compatible SPICE model for enhancement mode carbon nanotube field effect transistors," in International Conference on Simulation of Semiconductor Processes and Devices, pp. 166-169, 2006.

[25]Stanford University, 2014. Stanford CNFET Model. [Online] Available at: https://nano.stanford.edu/stanford-cnfet-model [Accessed 15 5 2014].

[26]J. Deng and H. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region," IEEE Transactions on Electron Devices, vol. 54, pp. 3186-3194, 2007.

[27]J. Deng and H. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part II: Full device model and circuit performance benchmarking," IEEE Transactions on Electron Devices, vol. 54 ,pp. 3195-3205, 2007.

Author Profile

NiloofarCharmchi received her B.S. degree in computer engineering from Ferdowsi University of Mashhad, Iran, in 2013. She is currently pursuing the M.S. degree in the School of computer engineering, University of Isfahan, Isfahan, Iran. Her research interests mainly focus on VLSI Implementation on Nanotechnology, Digital Arithmetic, Microprocessor Architecture and VLSI Hardware Design.

Mohammad Reza Reshadinezhad was born in Isfahan, Iran, in 1959. He received his B.S. and M.S. degree from the Electrical Engineering Department of University of Wisconsin, Milwaukee, USA in 1982 and 1985, respectively. He has been in position of lecturer as faculty of computer engineering in University of Isfahan since 1991. He also received the Ph.D. Degree in computer architecture from ShahidBeheshti University, Tehran, Iran, in 2012. He is currently Assistant Professor in Faculty of Computer Engineering of Isfahan University. His research interests are Digital Arithmetic, Nanotechnology concerning CNFET, VLSI Implementation, Logic Circuits Design, and Cryptography.