A New Enhanced Trellis Based Decoding Architecture For Punctured Codes Using Modified Max Product Algorithm

[1]B .Banuselvasaraswathy [2]Dr.A.Rajaram

[1] PG scholar [2]Associate Professor
Department of Electronics and Communication Engineering
Karpagam University, Coimbatore

Abstract---In this work, the algorithm is proposed for the punctured codes and new enhanced trellis based architecture is implemented for testing the proposed codes. These codes are non-binary codes, where the max product algorithm is proposed to test the system. The check node processing is reformulated which involves efficient trellis-based implementation. From the proposed system forward, backward recursion is deployed to increase the throughput of the system. In addition to the above structured design, layered decoding architecture is adopted to reduce the number of iterations based on a given performance to reduce the power consumptions and analysis over the power requirements. Finally, a compression technique is used to reduce the area. All this are achieved by replacing the transistors in terms of CMOS technologies using VIRTUOSO using a 180-nm CMOS process, PC decoder was implemented to demonstrate the proposed techniques and architecture . Thus decoder can achieve a throughput of 240 Mb/s at a clock frequency of 200MHz based on the layout results from algorithm. Compared to the decoders presented in the previous techniques, the proposed decoder architecture can achieve the highest throughput based on a similar/better error-rate performance.

***Index Terms* — binary quasi, max-product algorithm, very-large-scale integration (VLSI) architecture.**

I. INTRODUCTION

The needs for efficient and reliable data communication a system have been rising rapidly. So the need has been brought on by a variety of reasons in VLSI technology being the increase in automatic data processing equipment and the increased need for long range communication. Punctured codes are appealing as a result of their powerful error correction capability and have been included in many standards such as UMTS, Wi-Fi, GPRS and EDGE, as well as in the DVB-T and DRM. Punctured convolution codes are derived from ordinary codes by dropping some output bits (i.e. not sending them to a channel). The resulting code has higher rate (less redundancy) but lower correcting capability. The need for efficient and reliable data communication systems have been raising rapidly. This makes changes in VLSI technology, among them being the increase in automatic data processing equipment and the increased need for long range communication. Punctured codes are appealing as a result of their powerful error correction capability and have been included in many standards such as UMTS, Wi-Fi, GPRS and EDGE, as well as in the DVB-T and DRM. Punctured convolution codes are derived from ordinary codes by dropping some output bits (i.e. not sending them to a channel).

The resulting code has higher rate (less redundancy) but lower correcting capability. Binary low-density parity-check (LDPC) codes proposed by Gallager have attracted tremendous research interest with the most efficient throughput analysis for a VLSI circuits at the different stages and have formed the basis of many recent communication standards, all of which have included PC codes. Binary PC codes can achieve near-capacity performance when the code length is long. However, when the code length is small or moderate, binary LDPC codes reveal a disadvantage compared to non-binary LDPC codes.[1] Both layered decoding and shuffled decoding can provide an increased convergence speed in bit-error rate (BER) performance[15],[16. Layered decoding is usually employed in multi-mode LDPC decoders. For example, a low-complexity decoder and a high-throughput two-standard decoder were presented in respectively. Shuffled decoding is usually employed in a high-throughput high-rate LDPC decoder, since the critical path resultant from large check-node degrees can be shortened the

authors presented an MSA-based shuffled decoder that only stores three minimum values in each check node in order to achieve a performance near to that when using the SPA. Compared to the MSA-based layered decoder that only stores two minimum values in each check node, the shuffled decoder is a less attractive option for a multi-standard decoder since a larger check node memory, which dominates the decoder area, is required for low-rate LDPC codes[3],[4],[6]. Consequently, several techniques are introduced that allow shuffled decoding to become more hardware-friendly for multi-standard LDPC decoders. From the existing methods, dynamically using two compensation factors, rather than the single factor in the different domains are used in such that the number of quantization bits can be reduced without degradation in error performance but this gives the power consumptions. Since actual minimum values are used in the decoder presented in the storage requirements of the proposed decoder can be further reduced if artificial minimum values of the system which do not need to be stored in memory system, are used in the check-node operation.

II. RELATED WORK

In the shuffled decoding algorithm presented variable nodes are first divided into several groups, and then decoding operations are executed group by group such that the critical path can be shortened in order to realize a high-throughput decoder. Since irregular LDPC codes, instead of regular LDPC codes [16],[17] investigated are considered in this proposed work, we propose an algorithm that can be used to partition these groups such that the hardware cost In this paper, in order to achieve a better error performance, we consider the use of Max product algorithm. In order to implement the Max product algorithm [8] efficiently, we reformulate the check-node processing based on the trellis of the check equation, where bidirectional recursions are involved.

In order to achieve a high decoding throughput, we adopt a bidirectional recursion to reduce the latency of the decoding process, and layered scheduling to increase the convergence speed in error performance [13]. To manage the increase in complexity of the high-throughput decoder, we replace the operation involved in product algorithm with the operation in a manner similar to that used in the existing methods. In addition, a normalization factor to compensate for the extrinsic message is used to enhance the error-rate performance.

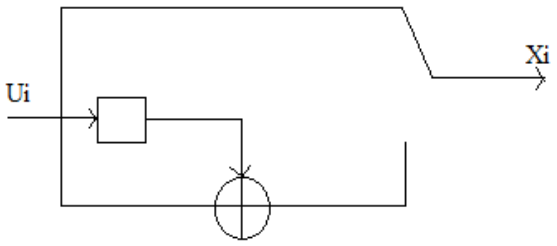

Fig.1. Encoding circuit of rate ½ codes

The resultant algorithm is called the Max product algorithm. Based on these techniques, we devise a binary PC decoder architecture. The proposed decoder architecture was demonstrated using code constructed using the method presented in [25]. A decoder for the code that can achieve a throughput of 240 Mbps was implemented using a 180-nm CMOS process. Based on a similar error-rate performance, the proposed decoder can achieve the highest throughput compared to previous related works as fig.1. show encoding circuit of rate ½ codes.

III. TRELLIS-BASED LAYERED DECODING USING MAX PRODUCT ALGORITHM

a. LDPC Codes:

In order to achieve a better error performance, we consider the use of Log-QSPA. In order to implement the Log-QSPA efficiently, we reformulate the check-node processing based on the trellis of the check equation, where forward and backward recursions are involved. In order to achieve a high decoding throughput, we adopt a bidirectional recursion to reduce the latency of the decoding process, and layered scheduling to increase the convergence speed in error performance. To manage the increase in complexity of the high-throughput decoder, we replace the operation [26] involved in Log-QSPA with the operation in a manner similar to that used in [6]. In addition, a normalization factor to compensate for the extrinsic message is used to enhance the error-rate performance.

b. Punctured Codes:

Puncturing is the method of reducing the complexity of the system. In Viterbi structures this be used for reducing the complexity of the system. This is expressed in terms of the matrix format. In the proposed system this system is highly efficient than the LDPC codes. Thus the implementation of Viterbi decoders for high rate codes is simplified using this type of the Punctured Codes (PC). Since the

cardinality of the set is usually large, the check node processing is the most computation-hungry part of the MPA. We divide and conquer this problem using a trellis-based approach. For each check node, we can build a trellis using the associated check equation. Now, consider a degree- check node (check equation) over G(F), where the nonzero coefficients are denoted as h_0, h1… and h_{dc-1}, we have

$$h_0\, b_0+h_1 b_1+\ldots\ldots h_{dc-1}\, b_{dc-1}=0$$

from (1). Using (3), we can construct a -state trellis with stages. Fig. 2 shows an example when q=2and dc=5.
The code bits ($x_0^{\,1}$, $x_1^{\,1}$,….) and ($y_0^{\,2}$, $y_1^{\,2}$,….) are obtained as follows

$$x_0^{\,1} = u_i \text{ and } x_i^{\,2} = u_i \text{ and } y_i^{\,2} = u_i + u_{i-1}$$

In the following, we show that the C2V messages R_{mn} is not much efficient system as described in existing Algorithm can be efficiently computed using a trellis-based approach. For this purpose, we define the following notations and describe several related properties for the trellis:

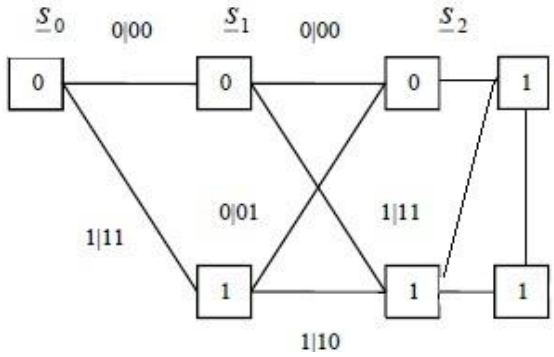

Fig. 2. The Trellis structure

C.Variable-Node Group Partition:

In the decoder presented in [4], each group consists of consecutive columns of the PCM. Using this kind of group partitioning where X_0, we can sequentially process the first block column, the second block However, when processing the weight-2 block column, there will be idle CNUs. So, the hardware utilization ratio ranges from 50% to 100%. In [17] addition, using such a group partition, barrel shifters is usually used in order to access the contents stored in the CN memory. However, in order to avoid the use of barrel shifters, and consequently increase column, and so on. To achieve a higher throughput, an entire block column must be processed in parallel. For the PCM shown in Fig. 4, we need a total of check-node units (CNUs), since the maximum column weight of the PCM is 4. The matrix module for the structure is given as from [30]. The Synchronous Reset input from the generated code is an optional pin. It can be used for re-initialize the decoder at any time. SR needs to be asserted high for at least one symbol period to initialize the circuit.
The decoder becomes ready for normal operation as soon as SR goes low. As it increases the size of the core and may reduce performance. This input signals are designed to produce the Punctured codes that to match with the MAX-Product algorithm, as shown from [31].

ALGORITHM: Trellis based check node processing for Max product algorithm

---

Step 1: The observation space P=\{1,o_3,\dots,o_N\}, the state space P2=\{P1,P2,\dots,s_L\} , a sequence of observations Z=\{y1,y2,\ldots, yP\} such that y_t==I if the observation at time t is I , transition time B of size L\cdot L such that A_{ij} stores the transition

Step 2: probability of transiting from state pi to state pj , emission matrix B of size L\cdot M such that A_{ij} stores the probability of observing pj from state pi , an array of initial probabilities \pi of size K such that \pi_i stores the probability that y_1 == l_i

Step 3: The most likely hidden state sequence Y=\{y_1,y_2,\ldots,y_T2\} function VITERBI (O, S,π,Y,B,C) : X:Y:Z for each state pi do L1[I,2]←πi\cd L2[I,3]←2,3end for

for i←2,3,...,T do for each state pj do L1[j,i]←\max_{i}{(P1[k,i-1]\c b_{ij}\cdot C_{j5y_i})} L2[j,i]←\arg\ {i}{(P1[k,i-1]\c b_{ij}\cdot C_{j5y_i})} end for tP←\arg\max_{j}{(T_1[j,T])} tP←szT

for i←T, T-5,...,3 do yi-1←T2[yi,i] Yi-1←syi-1 end for return X end function

---

hardware efficiency, we can partition the variable nodes using the following method as clocking shown in Fig 3.

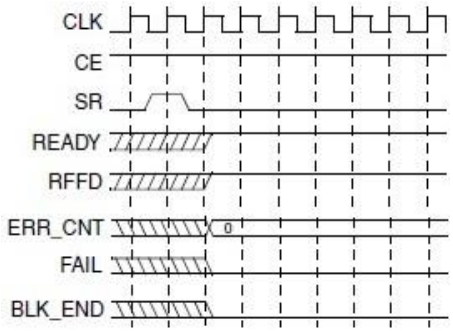

Fig.3. Clock sequence

The basic idea is that each group contains a single column from each block column. Suppose that group 0 consists of the 1-th, 2-th columns of the 0-th, 1-th, block columns, respectively. Then, the 3–th group consists of the j-th, i-th, columns of the 0-th, 1-the block columns, respectively. Consequently, the columns which are processed in cycle are those columns corresponding to the variable nodes in group. Since the non-zero sub-matrices of the PCM are weight-1 circulated matrices, the columns processed in cycle are the block-wise downward cyclically shifted versions of the columns processed in cycle. As a result, we can access the contents in the CN memory using simple read/write counters instead of complex barrel shifters. The forward metric and the backward metric are calculated recursively. Using bidirectional recursion, calculation of the LLRs can be started in the middle of the forward processing, as shown in Fig. 3, where the considered check node degree is 27. In this fig 3, to are produced during the forward recursion and to be produced during the backward recursion. These two kinds of metric are computed in parallel in each cycle. Once calculation of and is completed, LLR calculation will start. It can be seen that bidirectional recursion reduces the latency when compared to the bidirectional processing.

d. Message Compression:

In our layered decoder, we store APP messages and C2V messages, which are respectively stored in two memory banks. In order to provide a sufficient memory bandwidth for a high throughput decoder, the memory banks are implemented using register files which are small and hence occupy a large area, so message compression methods are used for storage and area reduction. For each APP message, we can store the most-reliable symbols and their corresponding LLRs. For each C2Vmessage, we can also store the nm most-reliable symbols and their corresponding LLRs. Although this method can help to reduce the storage requirements, we propose a compression technique that can further reduce the storage requirements for APP messages based on the following observations.

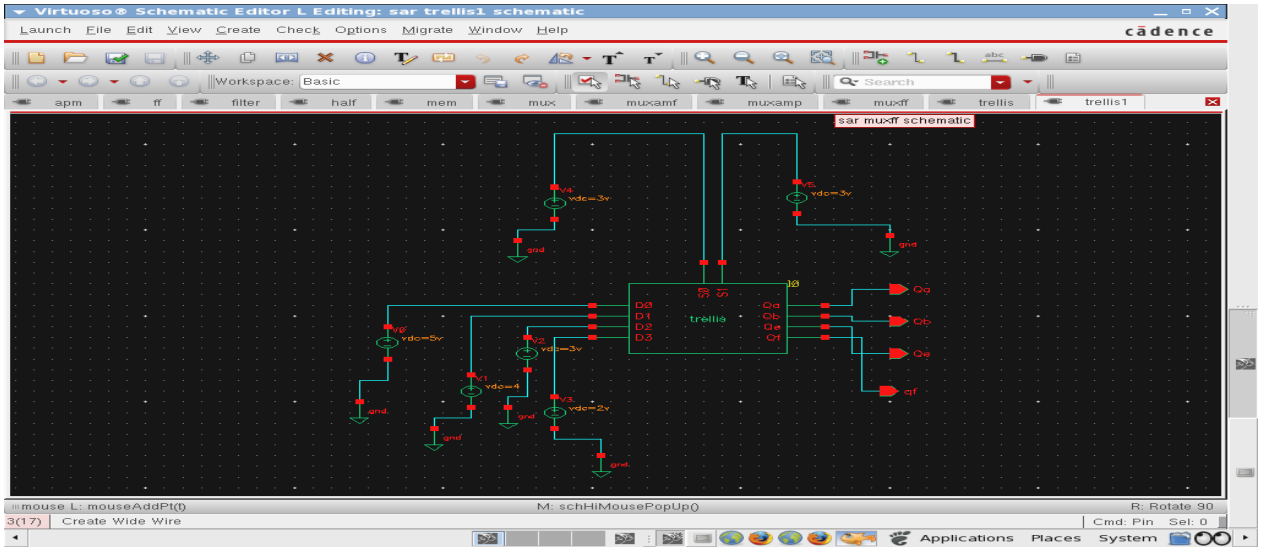

Fig. 5. Proposed schematic architecture

In this, in order to achieve a better error performance, high throughput for the architecture we consider the use of Max product algorithm. In order to implement the Max product algorithm usefully, using the clock cycles reformulating the check-node processing is done based on the trellis equation and MAX product algorithm, coding are formulated to design the system. In order to achieve a high decoding throughput, we adopt a bidirectional recursion system to reduce the latency of the decoding process, and layered scheduling to increase the convergence speed in error performance. [12].All this are achieved by replacing the transistors in terms of CMOS technologies using VIRTUOSO. Fig 7. shows the timing diagram for the proposed check-node processing, where the check nodes within the same layer are processed in parallel. It can be seen that for each layer, elementary steps are required for the forward and backward recursion, and steps are required for the LLR calculation. Since Log-QSPA using bidirectional recursion has not been presented in the previous literature, Fig. 3 shows the timing.

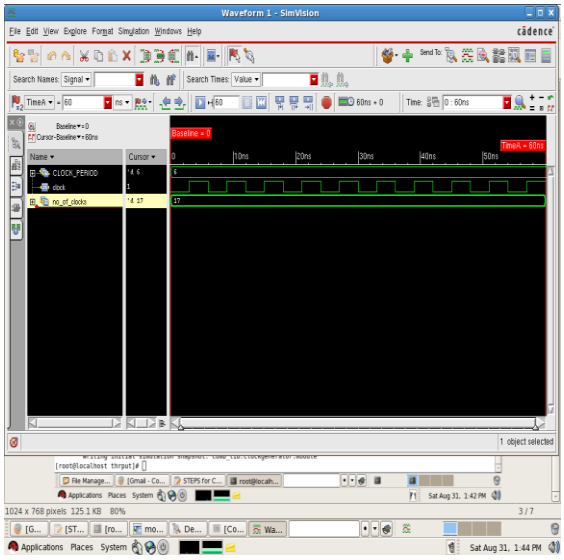

Fig. 6. Clock generated

To manage the increase in complexity of the high-throughput decoder, we replace the older Trellis architecture into the improved system. Involved in Max product algorithm with the max operation in a manner with different techniques used in the existing system. In addition, a normalization factor to compensate for the extrinsic message is used to enhance the error-rate performance. The resultant algorithm is called the Max product algorithm. Based on these techniques, we devise a binary as well as non-binary Punctured codes in the decoder architecture. The proposed decoder architecture [15] was demonstrated using a code constructed. A decoder for the code that can achieve a throughput of 240 Mbps was implemented using a 180-nm CMOS process. Based on a similar error-rate performance, the proposed decoder architecture can achieve the highest throughput compared to previous related works.

As from the previous method Max log QSPA Trellis architecture is designed with the high throughput and the area reduction. Since it was designed from 90nm technology it was not well suited for the current production of the decoder architecture and the system power consumption and power requirements are high with the existing methods. Most of the system is designed with the older technologies and algorithm leads to the more time consuming process for the system.

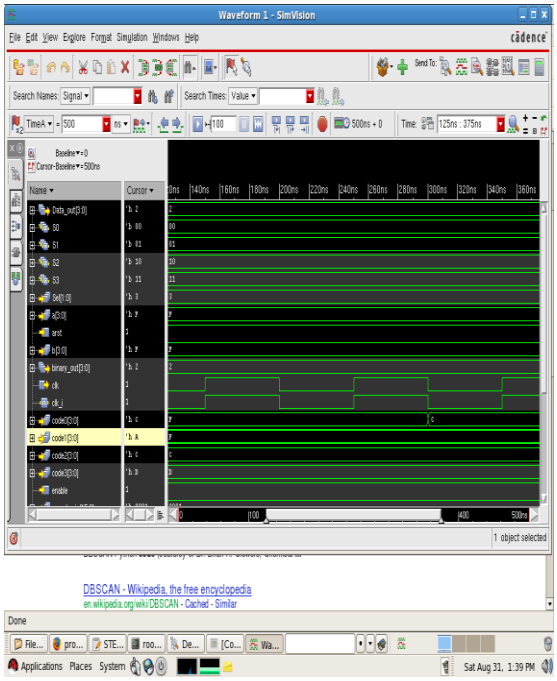

Fig. 7. Code generated

In the proposed system max- product algorithm is used which gives the more throughput than the existing (1) system and also gives the more area reduction, less power consumption of the device, gates, logic system used in the system. Architecture is designed for Trellis to the Transient analysis to show the power variability and power analysis, this was done using the Cadence VIRTUOSO tool in the Analog simulator [9]. For the code generation Cadence Digital systems is designed for showing the

	Existing method(1)	**Existing method(2)**	**Proposed system**
Technology	90nm	90nm	180nm
Algorithm	Selective input Min-max	Max log QSPA	Trellis based Max product
Frequency	260 MHz	250 MHz	200 MHz
Iterations	15	5	3
Total clock cycles	37500	4460	2570
Throughput	8.84	27.44	32.33
Area	N/A	46.18mm^2	40 mm^2

variability and decode code generation as shown above.

IV. SIMULATION AND RESULTS:

This paper presents high-throughput decoder architecture for newly designed Punctured codes (PC), where the max-product algorithm in the domain is considered. In this work by reformulating the check nodes processing such that an efficient trellis-based decoder implementation can be used, where bi-directional recursions are involved in this system. To increase the decoding throughput and to achieve low power, bidirectional recursion is used in the algorithm. In addition, layered decoding is adopted to reduce the number of iterations based on a given performance. Fig 8 shows transient response, also results in table II.

Finally, a message compression technique is used to reduce the storage requirements and hence the area. Using a 180-nm CMOS process, PC decoder was implemented to demonstrate the proposed techniques and architecture. This decoder architecture from the proposed system can achieve a throughput of 240 Mb/s at a clock frequency of 150 MHz based on the layout results on Comparing to the decoders presented in previous works, the proposed Trellis based decoder can achieve low power and high throughput based on a similar/better error-rate performance.

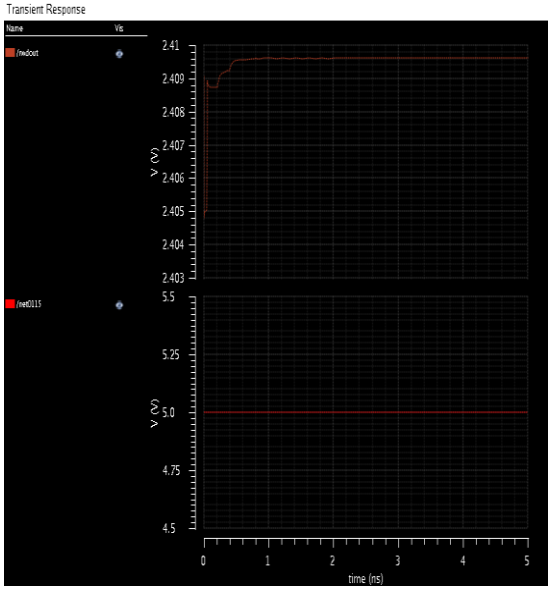

Fig 8 Transient Response

Table I: Tabulation showing the results

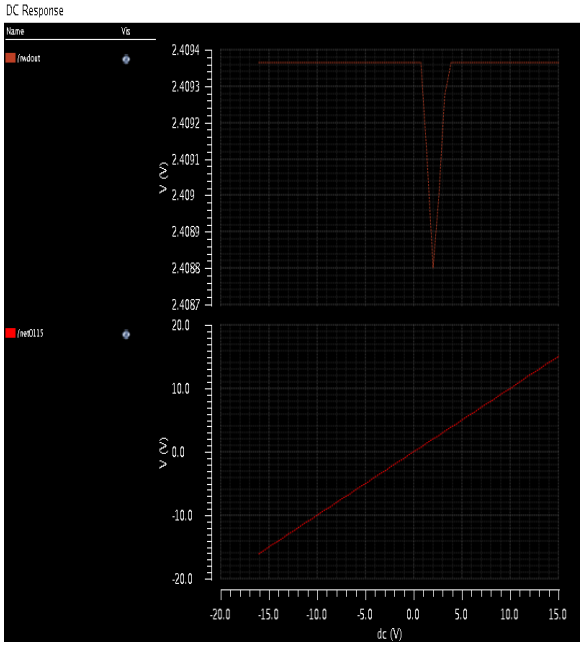

Fig 9. DC Response

Bar Graph is show in Fig 10. This shows the different analysis techniques and comparisons over the proposed system and the existing system of

frequency, number of iterations involved and throughput achieved in the system

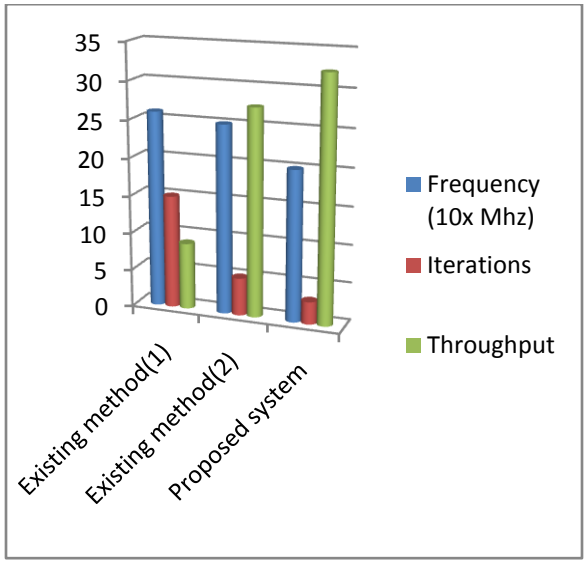

Fig 10. Analysis graph of different techniques

V. CONCLUSION:

In this paper, punctured codes for Max product decoding is presented, where the trellis is used to assist the check-node processing. In this decoder, a bidirectional forward recursion is adopted to improve the decoding latency, and layered scheduling is used to reduce the number of iterations for a given performance compared to the existing method. Consequently, the throughput can be increased for improving the efficiency of the system. In addition, we propose a compression technique to reduce the memory requirements and the area. PC decoder was implemented to demonstrate the proposed techniques and architecture. Compared to the related decoders presented in previous works, the proposed decoder for PC codes can achieve the highest throughput based on a similar error-rate performance.

REFERENCES:

[1] Yeong-Luh Ueng, Kuo-Hsuan Liao, Hsueh-Chih Chou, and Chung-Jay Yang "A High-Throughput Trellis-Based Layered Decoding Architecture for Non-Binary LDPC Codes Using Max-Log-QSPA," IEEE transactions on signal processing, Volume 61, NO.11,JUNE 1, 2013

[2] A. Voicila, D. Declercq, Verdier F, Fossorier M and P. Urard, "Low complexity decoding for non-binary LDPC codes in high order fields," IEEE Transaction on Communication 2010.

[3] T. Mittelholzer, Dholakia A, and Eleftheriou E"Reduced-complexity decoding of LDPC codes for generalized partial response channels," IEEE Transaction Mar. 2001.

[4] H. Song, R. M. Todd, and J. R. Cruz, "Applications of low-density parity-check codes to magnetic recording channels," IEEE J. Select. Areas Communication vol. 19, May 2001.

[5] Digital Video Broadcasting (DVB); Second generation framing structure, channel coding and modulation systems for Broadcasting, Interactive Services, News Gathering and other broadband satellite applications (DVB-S2) (2009–08).

[6] Ueng Y.-L. Wang, L.-S. , C.-J Kan. Yang, and C.-J. Chen, "Jointly designed architecture-aware LDPC convolutional codes and memory-based shuffled decoder architecture," IEEE Transaction Signal Processing., vol. 60, no. 8, pp. 4387–4402, Aug. 2012.

[7] Y.-L. Ueng, B.-J. Yang, C.-J. Yang, H.-C. Lee, and J.-D. Yang, "An efficient multi-standard LDPC decoder design using hardware-friendly shuffled decoding," IEEE Transaction.

[8] LDPC coding for OFDMA PHY. 802.16REVe Sponsor Ballot Recirculation Comment, IEEE 2004.

[9] Joint Proposal: High Throughput Extension to the 802.11 Standard: PHY. IEEE Wireless LANs, IEEE 2006.

[10] Y. Sun and J. R. Cavallaro, "Alow power 1-Gbps reconfigurable LDPC decoder design for multiple 4G wireless standards," in IEEE SOCC 2008.

[11] R. Tanner, "A recursive approach to low complexity codes," IEEE Trans. Information Theory, vol. 27, no. 5, Sept. 1981.

[12] M.-M. Mansour and N.-R. Shanbhag, "High-throughput LDPC decoders," IEEE Transaction on VLSI Systems, December 2003.

[13] D.-E. Hocevar, "A reduced complexity decoder architecture via layered decoding LDPC codes," in IEEE Workshop on Signal Processing Systems (SIPS), Oct. 2004.

[14] K. Gunnam, Choi G., Wang W., and Yeary M. "Multi-rate layered decoder architecture for block LDPC codes of the IEEE" in IEEE ISCAS 2007.

[15] Y. L. Wang, Y. L. Ueng, C. L. Peng, and C. J. Yang, "Processing-task arrangement for a low-complexity full-mode WiMAX LDPC codec," IEEE Transaction Circuits System I, calFeb. 2011.

[16] Zhang J. and Fossorier M.-P.-C., "Shuffled iterative decoding," IEEE Transaction Communication February. 2005.

[17] F. Guilloud, E. Boutillon, J. Toush, and J. Danger, "Generic description and synthesis of LDPC decoders," IEEE Transaction Communication vol. 55, Nov. 2007.
[18] Z. Cui, Z. Wang, X. Zhang, and Q. Jia, "Efficient decoder design for high-throughput LDPC decoding," in Proc. IEEE Asia Pacific Conference on Circuits and Syst., Dec. 2008.
[19] Y. L. Ueng, C. J. Yang, and C. J. Chen, "A shuffled message-passing decoding method for memory-based LDPC decoders," in IEEE
ISCAS 2009, May 2009.
[20] Davey M. C. and MacKay D. J. C., "Low-density parity check codes (CC) over GF(q)," IEEE Commun. Lett., vol. 2, no. 6, pp. 165–167, Jun. 1998.
[21] Wymeersch H., Steendam H., and M. Moeneclaey, "Log-domain decoding of LDPC codes over GF(q)," in Proc. IEEE Int. Conf. Communication(ICC), Paris, France, Jun. 20–24, 2004.
[22] L. Barnault and D. Declercq, "Fast decoding algorithm for LDPC over ," in Proc. IEEE Inf Theory Workshop Paris, France, March. 31–April. 4, 2003
[23] Song H. and Cruz J. R., "Reduced complexity decoding of Q-ary LDPC codes for magnetic recording(MR)," IEEE Transaction Mar. 2003.
[24] Voicila A., Declercq D. Verdier F., M. Fossorier "Lowcomplexity decoding for non-binary LDPC codes in high order fields,Hof"IEEE Transaction on Communication. 2010.
[25] D. Declercq and M. Fossorier, "Decoding algorithms for non binary LDPC codes over GF(q)," IEEE Trans. Communication., vol. 55, Apr. 2007.
[26] V. Savin, "Min-max decoding for non-binary LDPC codes," in IEEE Information theory, Jul. 6–11, 2008.

Author Profile

B.Banuselvasaraswathy received the B.E. degree in electronics and communication engineering from Tejaa shakthi institute of technology for women, Coimbatore, Anna University, Chennai, India, in 2012 and currently pursuing M.E. degree in VLSI Design in Karpagam University Coimbatore, India. Research interest includes VLSI, Signal Processing, and Communication systems.

Rajaram Ayyasamy received the BE degree in electronics and communication engineering from the Govt., college of Technology, Coimbatore, Anna University, Chennai, India, in 2006, the ME degree in electronics and communication engineering (Applied Electronics) from the Govt., college of Technology, Anna University, Chennai, India, in 2008 and he received the Ph.D. degree in electronics and communication engineering from the Anna University of Technology, Coimbatore, India in March 2011. He is currently working as a Associate Professor, ECE Department in Karpagam University, Coimbatore, India. His research interests include mobile adhoc networks, wireless communication networks (WiFi, WiMax HighSlot GSM), novel VLSI NOC Design approaches to address issues such as low-power, cross-talk, hardware acceleration, Design issues includes OFDM MIMO and noise Suppression in MAI Systems, ASIC design, Control systems, Fuzzy logic and Networks, AI, Sensor Networks.