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Simulation of A Three-Level Full-Bridge Zero-Voltage Zero-Current Switching Converter With Switching Modes

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Abstract: Three-level dc–dc converters making use of high frequency transformers are suitable for integration in solid-state solutions for applications in electric power distribution systems. This paper presents a soft switching technique for usein solid state solutions with reduced voltage stresses across the devises, allowing higher voltage operation. Three-level full-bridge dc-dc converters that enables zero-voltage and zero current switching of all the main power switches. It describes the main operational modes and design equations of the converter as well as provides simulation and experimental results to demonstrate the feasibility of the proposed ideas.

Index Terms— Dc-dc converters, soft switching, thyristors, Mosfets, IGBTs, GTO.

I. INTRODUCTION

As on May 2017 India generating 330GW in that 67% thermal, 14% Hydro, 17% Renewables, 2% Nuclear.In 2014 world top ten installed generations in GW China-1223, USA-1110, Japan 311, India 217, USSR 226, Germany 181, Canada 146, Brazil 129, France 126, and Italy 114GW.HIGH-VOLTAGE high-power isolated dc–dc converters have several potential uses in the electric utility industry, such as interfaces for high-power distributed generation, renewable resources, energy storage, dc interlinks, and solid state power substations[1-6]. Traditionally, switching devices with high-voltage blocking capability, such as thyristors and gate turn-off thyristors (GTOs) are used since they are more compatible with voltage levels seen in utility applications. The main disadvantage of these devices is that they switch very slowly, and in the case of thyristors, an external circuit is required for Turn OFF. Faster switching devices such as MOSFETs and (low voltage) insulated-gate bipolar transistors (IGBTs) bring many advantages in terms of system size and dynamic response but are unable to withstand large voltages. In order to take advantage of these smaller faster devices, several multilevel topologies have been proposed in order to reduce the voltage seen by individual switching devices. The main multilevel topologies-diode-clamped, flying capacitor, and cascade-provide for reliable division of voltage across the switching devices [1]. High efficiency is required for any high-voltage solid-state solution intended to replace fundamental-frequency transformers in utility applications since existing transformer technology can be as high as 99% efficient. Peak losses in switching converters occur during the switching instants, and these losses increase with increasing switching frequency. Many soft-switching topologies have been proposed to reduce these switching losses, with quasi-resonant phase-shifted zero-voltage switching (ZVS) and zero-voltage zero-current switching (ZVZCS) drawing particular interest since they do not cause added current or voltage stresses to the converter components. Of the two, ZVZCS is preferred due to the reduction of the circulating cur-rent and the wide-load operation ability. Over time, researchers combine d these soft switching topologies with multilevel topolo gies to provide superior performance at high voltages converters [1-6]. ZVS and ZVZCS three-level (3L) half bridge (HB) converters have been proposed, but these converters face the disadvantage that they only apply half the dc-bus voltage to the primary of the transformer. This paper presents a simple control strategy that reduces control complexity; device voltage stresses and achieves soft switching for all main power devices for the 3L FB ZVZCS converter topology. In addition, this converter has reduced circulating currents, wider load operation compared to the ZVS 3LFB, and the control can be implemented with existing phase shifted pulse width-modulated (PWM) controllers.

II. PROPOSED ZVZCS CONVERTER

The goal of the design is to produce a dc–dc converter that achieves soft switching for all the main switches, reduces the voltage stresses across each main switch, and controls the voltage on the secondary as per an FB step-down converter. Fig. 1 shows the circuit topology and the operational wave-forms of the proposed converter. The resistance R load equivalent resistance and might represent, for example, the inverter interfacing a distribution system. The intermediate

voltage stages typically available in a 3L converter (i.e., ±V/2) allow a better approximation of a sinusoid thus resulting in are deduction in harmonic levels for the inverter case, but this feature is not applicable to the dc–dc converter in this paper since the output voltage Vout, fixed at a constant dc level, is greater than the intermediate levels typical of dc–ac 3L converters. If the intermediate voltages were used, the voltage at the input of the diode-bridge rectifier would be less than V and the rectifier would not conduct, so no power would be delivered to the load. Table 1, gives the proposed switching states and identifies the voltage levels V S_{out} at the output of the transformer for each switching state. A "+" symbol indicates that the switch is ON during the switching state, while a "–" symbol indicates that the switch is OFF. The switching frequency is fixed and each switch is ON for exactly half a switching cycle, but the timing of the turn ON and turn- OFF of each switch is controlled so that the dc-bus voltage is applied to the transformer for the desired time as with phase-shifted PWM. Using Table I and recognizing that the rectifier causes the voltage at the output filter to be positive regardless of the polarity of the transformer voltage, the reader can realize that the system has the same general operating modes as a buck converter and will have the same differential equations.

The switching scheme, though it does not allow the intermediate voltage levels, does achieve soft switching for all the main devices, as will be shown in Section III. Furthermore, the loss of intermediate switching states is consistent with other 3L soft-switched designs. As previously discussed, the rectifier diodes D change the transformer voltage so that a positive voltage is Drec1–Drec4 change the transformer voltage so that a positive voltage is applied to the output filter regardless of the polarity of the transformer voltage; thus, the converter's operation can be defined in terms of half cycles with the voltage and current seen by the output filter L_f – C being the same for each half cycle. If the converter is in state 1 for duration D × To/2, where D represents the duty cycle and is a fraction between 0 and 1, then the average voltage at the rectifier will be V_{out} = D × Vdc/n where n is the turns ratio of the transformer. This provides the desired dc voltage conversion and shows that the system operates as a transformerized buck converter.

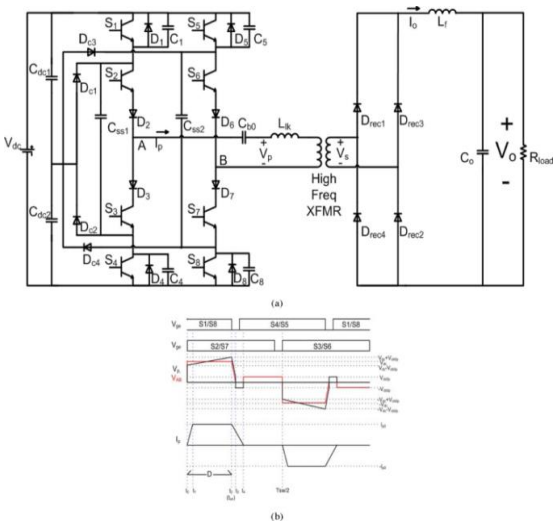

Fig. 1(a): ZVZCS Converter (b) Time

Table 1: Switching States -Voltage Levels

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	$V_{XFMR,S}$
1	+	+	-	-	-	-	+	+	V_{DC}/n
2	-	+	-	-	-	-	+	-	0
3	-	+	-	+	+	-	+	-	0
4	-	-	-	+	+	-	-	-	0
5	-	-	+	+	+	+	-	-	$-V_{DC}/n$
6	-	-	+	-	-	+	-	-	0
7	+	-	+	-	-	+	-	+	0
8	+	-	-	-	-	-	-	+	0

III. ZVZCS OPERATION METHODS

The equivalent circuit for the first five of the ten operational modes since the sub- sequent five modes operates similarly to the first five modes, along with the sixth operational mode to show its similarity to the first. The following analysis assumes that the switching devices are ideal; the output filter is large enough to act as a constant current source for the entire period and the blocking capacitor is large enough to act as a constant voltage source while the current is being reset.

Design Equations

The design of the converter involves determining values for, and the output filter. The output filter should

be large enough to maintain the load current for the entire switching period T C_{dc1}, C_{dc2}, C_{ss1}, C_{ss2}, C_1, C_4, C_5, C_8, C_{b0}, L_{lk}, while the transformer leakage inductance L should be minimized in order to minimize the reset time. Beyond these restrictions, transformer and filter design principles also apply. Capacitors $C_{dc1}$and C_{dc2} are essential for the proper voltage division across the switching devices. Consequently, they should be selected with identical values using tight tolerance parts. In practice, the dc-bus capacitors will be required to maintain the voltage through changes in the input voltage V and through voltage spikes caused by parasitic inductances, so a large value may be required. Smaller capacitors with good high-frequency response may be placed in parallel with the bulk dc-bus capacitors in order to handle high-frequency ripple due to parasitic components. Capacitors C_{ss1} and C_{ss2} dc are also identical. Fig. 2 shows that they conduct during mode 3 and its mirror, mode 8. These capacitors must maintain a near-constant voltage during the entire cycle; thus, they should be selected so that they do not experience more than a 5% voltage change during mode 3. Each capacitor conducts I/2 during mode 3, and its nominal voltage is $V_{dc}/2$. Therefore, the capacitor value required for a 5% ripple is

$C_{ss}= I_{p0}\times$ (t) 0.05 × V

This can be simplified using [6], so that

$C_{ss}= C_{r3} – t_{dc}$ 0.05 = 20× C

The size of the parallel capacitors,

C_{2rr} and S turn OFF, is determined by the minimum requirement to achieve ZVS during turn OFF, which requires that the parallel capacitors must be large enough to hold the voltage close to zero during the current fall time of the 8, which can be determined from the data sheet.

III. RESULTS AND DISSUCTIONS

The operation of the 3L FB ZVZCS converter was analyzed. Experimental results further demonstrated the feasibility of the proposed ideas in Fig 2 to 10.

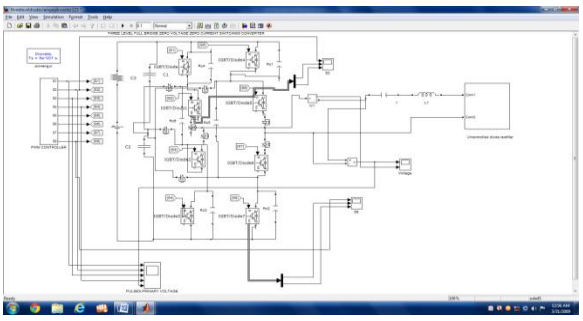

Fig 2: 3 level full Bridge dc-dc converters

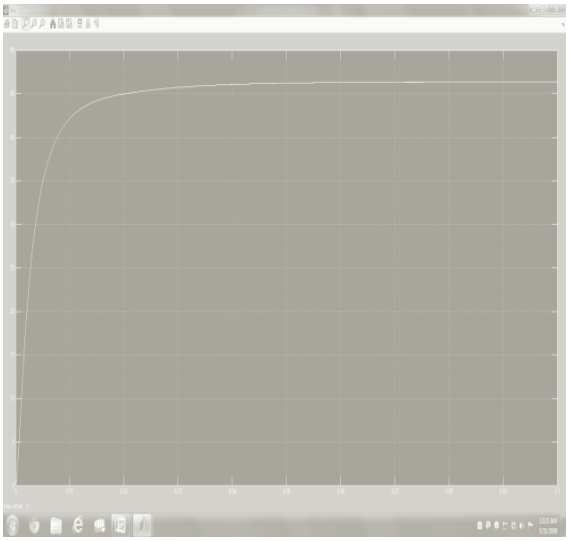

Fig 3: Output voltage of 46.5V DC

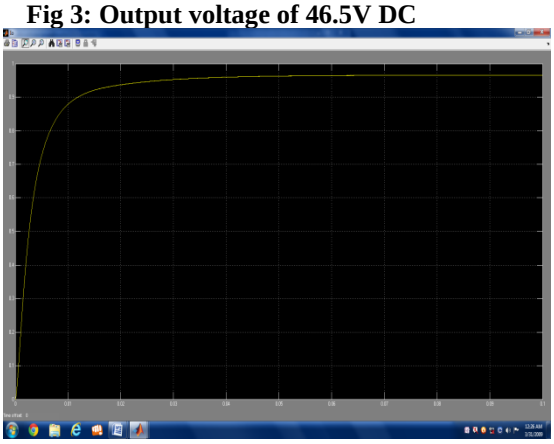

Fig 4: Output current of 1A DC

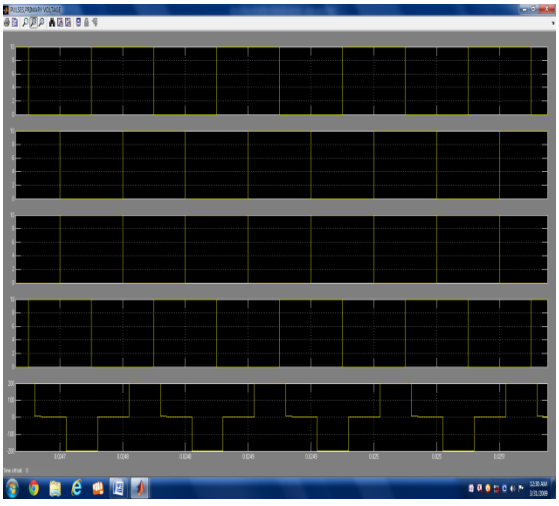

Fig 5: Pulses across switches and voltage

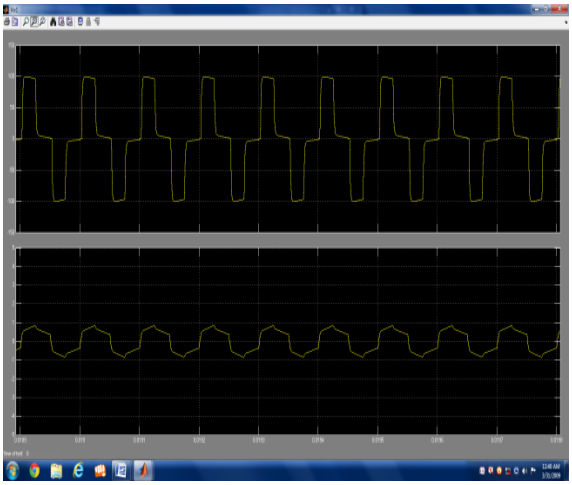

Fig 6: 3 level output voltage and current

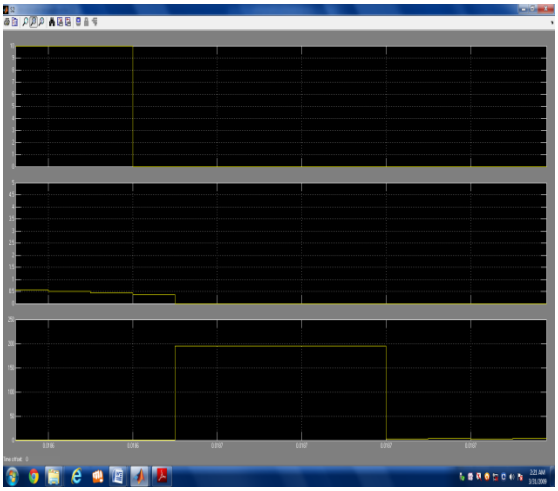

Fig 7: ZCS turn off of S_2 at full load and light load

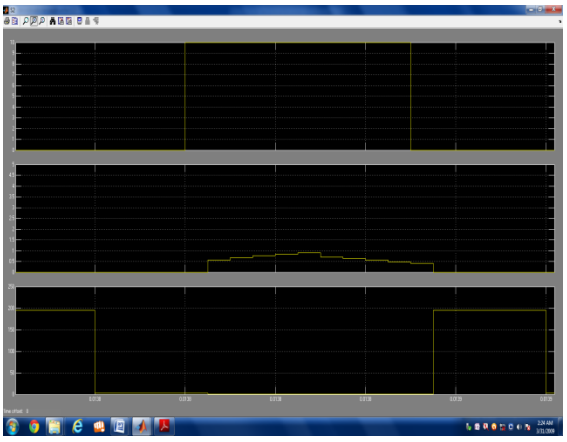

Fig 8: ZCS turn on at light load and full load

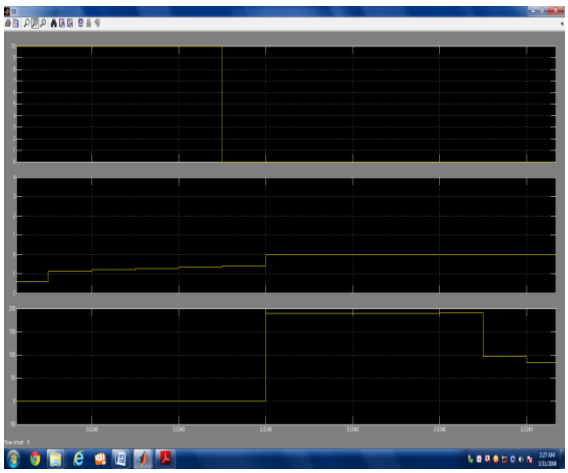

Fig 9: ZVS turn off of S_8 at light load and full load

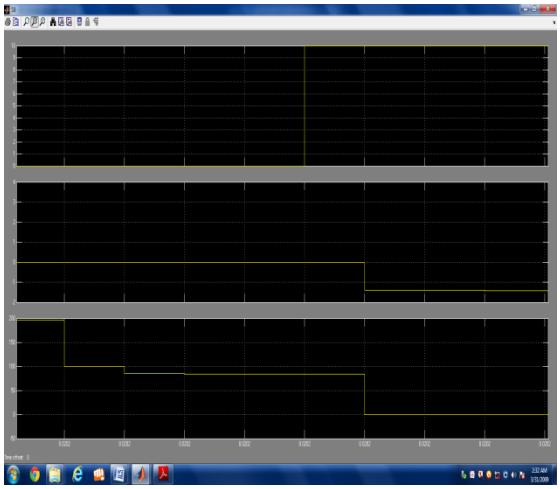

Fig 10: ZVS turn ON of S_8 at light load and full load

CALCULATION PART:
f_{sw} is switching frequency
E_{ZVS} off is voltage across switch when ZVS manner off
P_{ZVS}, off is Power losses across the switch
E_{ZVS}, off = 9.965×10^{-4} volts
P_{ZVS}, off = $4 \times E_{ZVS}$, off $\times f_{sw.}$ The switching losses at different frequencies are presented in Table 2.

Table 2: Switching Losses at Different Frequencies

S.No	Freq (KHz)	Power losses (w)	η(%)
1	10	20	95.83
2	15	59.79	87.5
3	20	79.7	83.33
4	25	99.65	79.23
5	30	199.3	58.47

V. CONCLUSIONS

This paper proposed a 3L ZVZCS converter with a simplified switching scheme for use in solid-state solutions. The converter was shown to have the advantages of soft switching and reduced voltage stresses across the devices, allowing higher voltage operation. Future research would include designing a prototype to implement an active clamp to reset the current thus eliminating the series diodes and the losses associated with them. This would have the added benefit of reducing the spikes from the rectifier diodes when the dc voltage is applied during modes 1 and 6.

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