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Ring Oscillator frequency measurement using improved delay equation.

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Abstract:

This work emphasis the problems in obtaining an accurate equation for calculating the delay of a CMOS inverter and provides a suitable solution. Propagation delay equation is employed in numerous applications, such as obtaining the oscillator frequency of a ring oscillator, whose accuracy is very important. The derived equation is tested for its accuracy and verified using simulated results. A comparison is made between the conventional and improved equation. The proposed technique was employed in cadence virtuoso TMSC 45nm and 180 nm technology and verified through the spectre simulator.

Key words: CMOS inverter, Ring oscillator, Propagation delay, Delay interval.

Introduction:

Oscillators are electronic circuit that produces periodic, oscillating signals which may be a square wave or a sine wave. Clock generation is the important function of Oscillators in digital systems. Ring oscillators are preferred rather than other oscillators because of its simplicity of architecture, ease of implementation, capability of oscillating at high frequencies, integrated nature and compatibility with different standards. The architecture of N-Stage schematic diagram shown in figure 1.Single ended ring oscillators (otherwise known as inverter based ring oscillator) consist of odd number of inverter stages in a loop, the feedback is given to the first stage from the final stage output. Output signal period of the ring oscillator depends on the number of intermediate stages, and the time delay td occurring in each stage. Equation (1) determine the frequency of the N-stage ring oscillator is given by [6],

$$f = 1/2Nt_d \quad (1)$$

Where, N is the number of stages in the ring oscillator. Propagation delay equation for a CMOS inverter is defined in the time interval between $V_{in} = V_{dd}/2$ and $V_{out} = V_{dd}/2$. The time delay occurring in CMOS inverter occurs during High-Low (tdHL) and Low-High transition (tdLH). So, an improved equation is devised to improve the performance of the propagation delay equation.

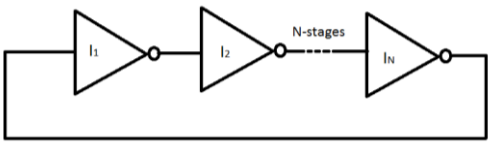

Figure 1: Schematic diagram of a Single ended Ring oscillator.

The delay is calculated using this equation and then the frequency of the ring oscillator is calculated with the help of the obtained results. The main aim of our work is to eliminate the simplifying assumptions in the conventional equation and make the new propagation delay equation more accurate. For this a detailed study about the delay time in the single ended CMOS inverter is made. The cause for inaccuracies are identified and eliminated.

Conventional technique:

Initially the frequency characteristic of the ring oscillator was analysed on the basis of 3 parameters namely, the number of stages , capacitance at each stage and the resistance. This estimation was done using Barkhausen's condition [1]. In [2], a new propagation delay equation is calculated in which the changes of the operating area of transistors are considered. Then in later period of time an analytical equation was derived to determine the oscillation frequency of a high frequency ring oscillator. This is given by [3],

$$f = \frac{Iss}{2NVsw(Cin + Cgd_p + Cdb_n + Cgdov_n + Cdb_p)} \quad (2)$$

This equation included time varying parasitic. The next method was analysing the transient response and delay in a nano-scale inverter [4]. This method helped to find out the time response, capacitance and supply voltage value. Then a devised a model to determine the delay of the inverter using DC transfer characteristics of the CMOS inverter [5]. Which was then followed by the differential equation calculation, devising a RC model of the circuit and based on average currents.

Proposed technique:

In this section we are going to calculate a more accurate equation for tdHL and a similar approach is used to calculate the value of tdLH. **i)** Input / output voltage curve,

The capacitance in Figure2 is considered as equivalent capacitance as it is composed of all the parasitic capacitance (drain diffusion, gate, drain-gate and wiring capacitance). In the following section the important timings and four regions are defined along with their features.

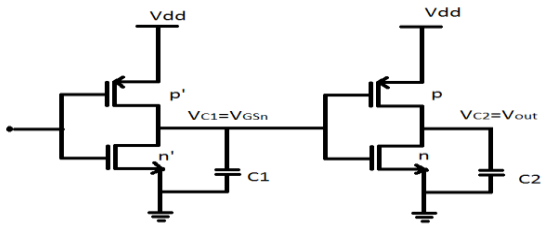

Figure 2: Two cascaded inverter stages with their parasitic capacitance (C1 and C2 represents the equivalent capacitance of all the parasitic capacitance of the transistors and the wiring).

In the following equations n, p, L and S denotes transistor n, transistor p, linear and saturation operating areas respectively.

t-1: Time at which the transistor n turns on.

t0: The beginning of time delay (t=0).

t1: The time at which transistor p turns off.

t2: The time at which transistor n enters the linear region.

tdHL: The end of delay interval.

With reference to [7] the equation for current and voltage equations of various regions is derived.Figure3 gives the I/O characteristics of the inverter.

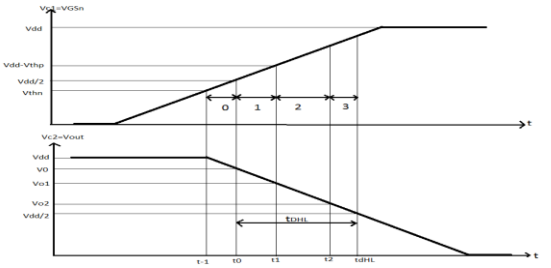

Figure 3: Input/output voltage curve of second transistor.

Region 0: At the beginning of this region C2 starts to discharge as Vc1 reaches Vthn. Both p and n transistors are on, since Vc1 is not high enough to turn off transistor p. Transistor n and p are in saturation and linear regions respectively. The bounds of voltages and times are given by [7],

$$V_{thn} < V_{c1} < \frac{V_{dd}}{2}, V_{dd} < V_{c2} < V_0, t_{-1} < t < t_0, t_0 = 0 \quad (3)$$

Then we determine VGSn0 and VSGp0. Gate-source voltages of the transistor are determined used the averages of the initial and final voltages.

Region1: This is the beginning of delay time where Vc1 is equal to Vdd/2. At the end of this region transistor p turns off as Vc1 reaches Vdd-|Vthp|, thus the transistor p and n are on and are in saturation region. The bounds of voltages and time are given by [7],

$$\frac{V_{dd}}{2} < V_{C1} < V_{dd} - |V_{thp}|, V_0 < V_{C2} < V_{01}, 0 < t < t_1 \quad (4)$$

Region2: At the beginning of this region only transistor is effective, as the value of Vc1 becomes equal to Vdd-|Vthp|. At the end of this region n enters linear region.The time and voltage bound is given by [7],

$$V_{dd} - |V_{thp}| < V_{C1} < V_x, V_{01} < V_{c2} < V_{02}, t_1 < t < t_2 \quad (5)$$

Region3: At the beginning of this region transistor n enters linear region. When this region ends Vc2 reaches Vdd/2. If n transistor does not enter the linear region, region3 is a part of region2. The bounds of voltages and times are [7],

$$V_x < V_{C1} < V_{dd}, V_{02} < V_{C2} < \frac{V_{dd}}{2}, t_2 < t < t_{dHL} \quad (6)$$

VGSn is close or equal to Vdd, hence we choose the value of VGSn3 as, $V_{GSn3} = V_{dd}$

After diving the delay interval and analysing their features, it is seen that the conventional equation is more simplified and numerous assumptions are made and many details are neglected. From Figure 3 a following conclusion can be made regarding the above discussions,

$$t_{dHL} = t_1 - C_2\left(\frac{V_{02} - V_{01}}{I_{nS2}}\right) - \frac{c_2}{\beta_n (V_{GSn3} - V_{thn})} \times \ln\left[\frac{\frac{V_{dd}}{2} \times (2(V_{GSn3} - V_{thn}) - V_{02})}{(2(V_{GSn3} - V_{thn}) - \frac{V_{dd}}{2}) \times V_{02}}\right] \quad (7)$$

There are three unknown values t1, Vo1 and Vo2 which are evaluated in [7] If we assume that |Vthp|= Vthn= Vth, the propagation delay equation will be,

$$t_{dHL} = \frac{C}{\beta_n} \times \left(\frac{\ln\left(\frac{V_{dd}}{2|V_{thp}|}\right)}{R(V_{dd} - |V_{thp}|)} + \frac{2}{(V_{dd} - \frac{|V_{thp}|}{2} - V_{thn})^2} \times \left[V_{thn} + \frac{(\frac{V_{dd}}{4} - \frac{V_{thn}}{2})^2 (e^{\frac{-2(\frac{V_{dd}}{2} - V_{thn}) \frac{3V_{dd}}{4} - \frac{V_{thn}}{2} \cdot |V_{thp}|)}{(V_{dd} - |V_{thp}|)^2}} - 1)}{(\frac{3V_{dd}}{4} - \frac{V_{thn}}{2} - |V_{thp}|) 2R}\right.\right.$$

$$\left.\left. - \frac{\ln\left(\frac{V_{dd}}{2|V_{thp}|}\right)}{2R(V_{dd} - |V_{thp}|)} ((\frac{3}{4}V_{dd} - \frac{|V_{thp}|}{2} - V_{thn})^2 - R(\frac{V_{dd}}{4} - \frac{|V_{thp}|}{2})^2)] - \frac{\ln[\frac{V_{dd}}{(3V_{dd} - 4V_{thn})}]}{(V_{dd} - V_{thn})}\right) \quad (8)$$

Where,

Vthn: Threshold voltage of N-transistor.

Vthp: Threshold voltage of P-transistor.

Equation (15) is the improved accuracy propagation delay equation. We have included the effect of both NMOS and PMOS transistors in the inverter, the variations in the gate-source voltage and their operating areas. Simplifying the delay equation,

$$t_{dHL} \approx \frac{CV_{dd}}{\beta_n (V_{dd} - \frac{3V_{th}}{2})^2} \qquad (9)$$

A similar approach is used to calculate the value for Low to High propagation delay equation. It is given by,

$$t_{dLH} = \frac{C \ln(\frac{V_{dd}}{2V_{th}})}{\beta_n (V_{dd} - V_{th})} + \frac{2C}{\beta_n (V_{dd} - \frac{3V_{th}}{2})^2} \times [V_{th} + \frac{R(\frac{V_{dd}}{4} - \frac{V_{th}}{2})}{6} (e^{\frac{-3(\frac{V_{dd}}{2} - V_{th})}{(V_{dd} - V_{th})^2}} - 1)$$

$$- \frac{(9R-1)(\frac{V_{dd}}{4} - \frac{V_{th}}{2})^2 \ln(\frac{V_{dd}}{2V_{th}})}{2(V_{dd} - V_{th})}] - \frac{C \ln[\frac{V_{dd}}{(3V_{dd} - V_{th})}]}{\beta_p (V_{dd} - V_{th})} \qquad (10)$$

Simulated results:

In this section we compare the proposed and conventional technique by implementing in 180nm CMOS technology, using a 9-stage ring oscillator. Figure 4 shows the layout design of 9-stage Ring Oscillator implemented in 45nm technology. The accuracy is checked for 180nm technology, this can also be implemented in 45nm technology. Figure 5 shows the schematic of 9-stage ring oscillator. The maximum power consumed by the ring oscillator with 9-stages implemented in 180nm technology is 1.44mW and occupies an area of 1504.1456nm^2.

When implemented in 45nm technology it consumes a maximum power of 184.4 μW with very minimum delay compare to the circuit implemented in 180nm technology. Out3 in figure 6 shows the 4th stage delay of the Ring Oscillator. Considering the proposed equation effect of various parameters on propagation can be calculated. Figure 7 shows the transient response of 9-stage RO implemented in 180nm technology and simulated using spectre simulator. We have also discussed the behaviour of the propagation delay equation in detail.

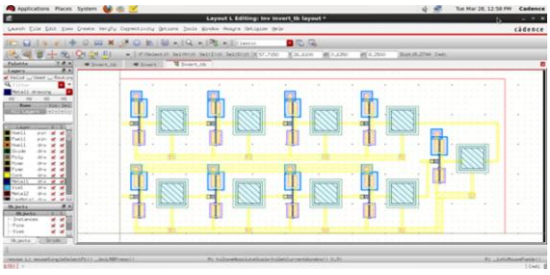

Figure 4: Layout for 9-stage ring oscillator in 180nm technology.

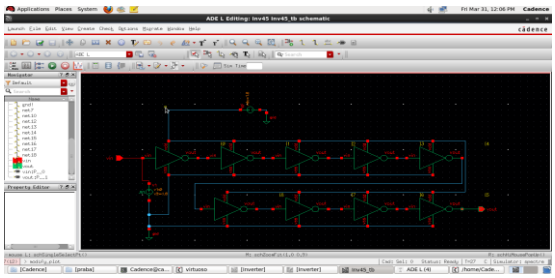

Figure 5: Schematic diagram of 9-stage RO implemented in 45nm technology.

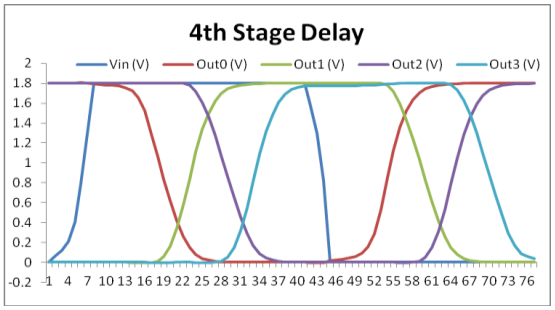

Figure 6: Shows the propagation delay analysis for four inverter stages.

Error percentage can be calculated using,

$$*Error = \frac{t_{d\_sim} - t_{d-proposed}}{t_{d-sim}} \times 100$$

$$**Error = \frac{t_{d-sim} - t_{d-conv}}{t_{d-sim}} \times 100$$

$$***Error = \frac{t_{d-proposed} - t_{d-conv}}{t_{d-proposed}} \times 100$$

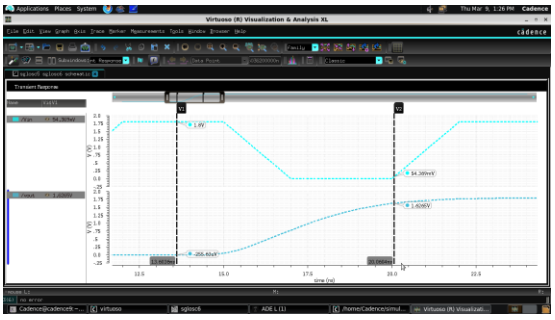

Figure 7: Transient response of 9-stage RO.

Conclusion:

The equation derived above is used to calculate the frequency of the single ended ring oscillator. This equation is derived to overcome the intricacies in the conventional equation. This equation gives more accurate results than the conventional equation. The conventional equation always under-estimates the value of delay, because in conventional equation the input voltage of the inverter is assumed to be ideal step function. The above analysis shows that implementing in 45nm technology is more efficient.

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