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BIST for arrays of wordorganised RAMs

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Abstract- Transparent Built InSelf-Test for word oriented RAMs produces test data with high degree of symmetry. Transparent test approach is applied to the idle state of systems. Reducing the test time is very important for avoiding the interrupt of testing. Transparent word oriented March tests are directly obtained by repeatly executing the corresponding bit oriented march test on each bit of word. In this system RAMs are of different size are used and each has different width structure. Finally analyze the fault word by using RAM structure in online condition

I. INTRODUCTION

Nowadays Built InSelf-Test for memories has become standard industrial one, since it has taken major part of the die area up to 94% by 2014.RAM modules are tested both after manufacturing and periodically in the field. During testing, a number of tests are applied to check that the RAM operates normally.

A March test consists of number of march elements that perform a preset sequence of read and or write operation for every word. Conventional March algorithms [5]-[7], starts with the beginning of write all –zero phase where all RAM cells are initialized to '0'. TestingofRAMmodulesisperformed Bothrightaftermanufacturingandperiodicallyinthefield.Duringmanufacturingtesting,variouskindsoftestsareappliedinordertoensurethattheRAMoperatesnormally.AMarchtestcomprisesaseriesofmarchelementsthatperformapredeterminedsequenceofoperations(readand/orwrite)ineveryword.Traditionalmarch algorithmstartwithaninitialwrite-all-zerophase,wherealltheRAMcellsresetto'0'inordertoensurethatthefinalsignatureintheoutputcompactoris known.

Normally testing is distinguished into start up testing and online testing. Startup testing is performed during start of the system and be appear manufacturing testing. Online testing means testing during normal operation, where the normal operation of RAM comes to be stop and it becomes difficult to shut down the system and it makes the advantage of that the contents of RAM cannot be lost. These kinds of testing are useful for space applications, wireless sensor, network nodes etc.

Soft errors can be deal during operation of the system, addingstandard online checking based on error detectingCodes. For detection the certain types of error can be vouch. But error detection can be done only during read operations, the time between the occurrence of error and its detection, referred to as error detection latency, it may be very high. For examplein the application of telecommunication switching, it is unable to detect a large amount of data, when the data are needed. In opposition, errors should be detected easily, before the data are needed by the system. In addition, errors error detection increases the number of check bits which in turn increases the hardware overhead.

In order to overcome the problems in transparent BIST, signature prediction phase is used and write all zero phase is neglected, during which signature is captured and stored. The final signature is compared against the captured one to check whether the fault has present in the RAM word or not. The majorProblems encountered in transparent BIST are test pattern generator and response compactor. To verify the correct operation of memory it is necessary to apply the single signal to the inputs of data bus and two gates (one AND and one OR). The need to capture the contents of the data in memory at the beginning of transparent BIST test imposes the need to employ Multiple Input Shift Registers(MISR) structures, increasing the hardware overhead.

In Symmetric Transparent BIST, the signature prediction phase is skipped and the march series is modified in such a way that the final signature is equal to all zero state, irrespective of the RAM initial contents. For bit organized RAMs Single Input Shift Registers(SISR) was used whose polynomial switches between a primitive polynomial and its reciprocal for different march elements of march series. Multiple Input Shift Registers (MISR)are used in word organized RAMs whose characteristics polynomials is modified in a fashion that can serve as response compactor. This scheme requires the modification of existing registers in order to serve as response evaluators and requires control logic to switches between different polynomials during the march series.

The advantage of using RAM modules in the circuit has lower hardware overhead and eliminates the need of multiplexers in the circuit path. In Symmetric Transparent RAM BIST, the compaction and data generation module was implemented by using an ALU. The output of RAM is given directly to the inputs of ALU or by using processor instructions. This scheme imposes lower hardware overhead and less complexity than previously proposed scheme.

In order to test memories of the same word width in a transparent way, one can use transparent BIST in a moving manner. This scheme cannot be apply to test memories having different word width. Hence this requires separate BIST modules and increases hardware overhead. A Symmetric Transparent Online BIST for Arrays of Word organized RAMs are proposed. This scheme uses an ALU to generate test patterns and compress the response of memory modules, the word width of memory can be smaller than number of stages in ALU. Hence multiple non identical memories are tested in a pipeline fashion and the area cost is reduced.

Notation	Meaning
R_a	ReadthecontentsofawordoftheRAM,expectingtoreadtheinitialcontentsoftheRAMword(i.e.beforethebeginningofthetest)
r_a^c	ReadthecontentsofawordoftheRAM,expectingtoreadthecomplementoftheinitialcontentsoftheRAMword
$(r_a)^c$	ReadthecontentsofawordoftheRAMexpectingtoreadtheinitialwordcontentsandfeedthecomplementvaluetothecompactor
w_a	Writetothememoryword;thevaluethatwasstoredin thismemorywordatthebeginningofthetestis(assumedtobe)wr
W_a^c	Writetothememoryword;theinverseofthevaluethatwasstoredinthismemorywordatthebeginningofthetestis(assumedtobe)writtentotheword.

II PREVIOUS APPROACHES

AmarchalgorithmconsistsofnmarchelementsdenotedbyMi,with0 ≤i<n.Eachmarchelementcompriseszero(or more)writeoperations, denotedby w0/w1meaningthat0/1iswrittentotheRAMcell,andzero(ormore)readoperationsdenotedbyr0/r1, meaning that0/1isexpectedtobereadfromthememorycell.InMarch algorithm↑denotesanincreasingaddressingorder(whichcanbeany arbitraryaddressingorder)and denotesadecreasingaddressingorder (whichistheinverseaddressingorderof↑).
Traditionalmarchalgorithmserase thememorycontentspriortotesting;therefore,theydonotserveasgoodplatformsforperiodicBIST. In transparentBISTwheretheinitialw0phaseisbypassed,anda "signatureprediction"phase issuedinstead.Thesignaturepredictionphaseconsistsofreadoperationsanditisutilizedinordertocalculateasignaturethatwill becompared against the compacted signaturecalculatedduring the(remaining)marchtest.Thenotationforthetransparentversions ofthealgorithmsdiffersfromtheoneusedintraditionalmarch algorithms.Insteadofr0,r1,w0, w1,thenotationsr_a,r_a^c,w_a,$w_a^c$and$(r_a)^c$areutilized,asclarifiedinTable1.
Thedatadriventothecompactorwith the$(r_a)^c$operationareidenticaltothedatadrivenbyther$_a^c$.The importance of the $(r_a)^c$operation is during the signature prediction phase the contents of RAM are equal to the initial contents; therefore, in order to simulate the r_a^coperation thesecontents are inverted prior to entering the compactor.

Table 1: Notations for symmetric transparent BIST

Word organized memories are tested by using Multiple Input Signature Registers and by toggling between a primitive polynomial and its reciprocal one during the ↑ read and ↓ read operations, the final signature is equal to the all zero state.

III. PROPOSED METHODOLOGY

The drawbacks of existing system are, in transparent BIST the signature prediction phase adds the total testing time up to 30% and separate BIST modules are used for each RAM which increases the hardware overhead.
In transparent BIST the content of the memory at the end of the test is identical to before the test. Since the read elements of signature prediction phase is identical to the read elements of the testing phase. But in my proposed work, more than one memory with varying word widths are used when the number of stages of the ALU is larger than the memory word width. The block diagram and flow diagram of the proposed methodology are shown in fig 1 and 2.
First, the number of bits in the RAM isinitialized. Here, RAMs of different word widths are used. By creating the rules, the fault addresses are checked by using BIST. From that, row and column address information from BIST are predicted. These faulty addresses are copied to RAM arrays. The next block is March test. The test is marching through memory. From these, all these information are fed to solution stage by multiplexing all the address separate for rows and columns.
The next block is extract march bits. March 1 bit begins by writing backgrounds of 0s then read and write back complement values for all cells. Marching-0 follows exactly the same pattern, with the data reversed. The next block is checking error and finally each possible solution one and thus do not require the parallel sub analyzers are evaluated. This form gives the easiest way to predict solution for faulty address.

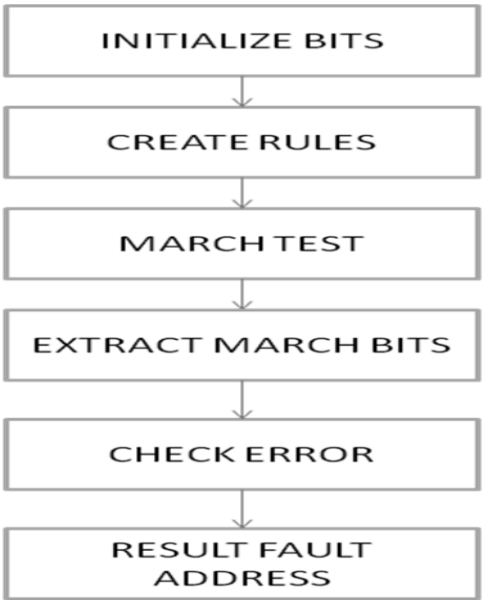
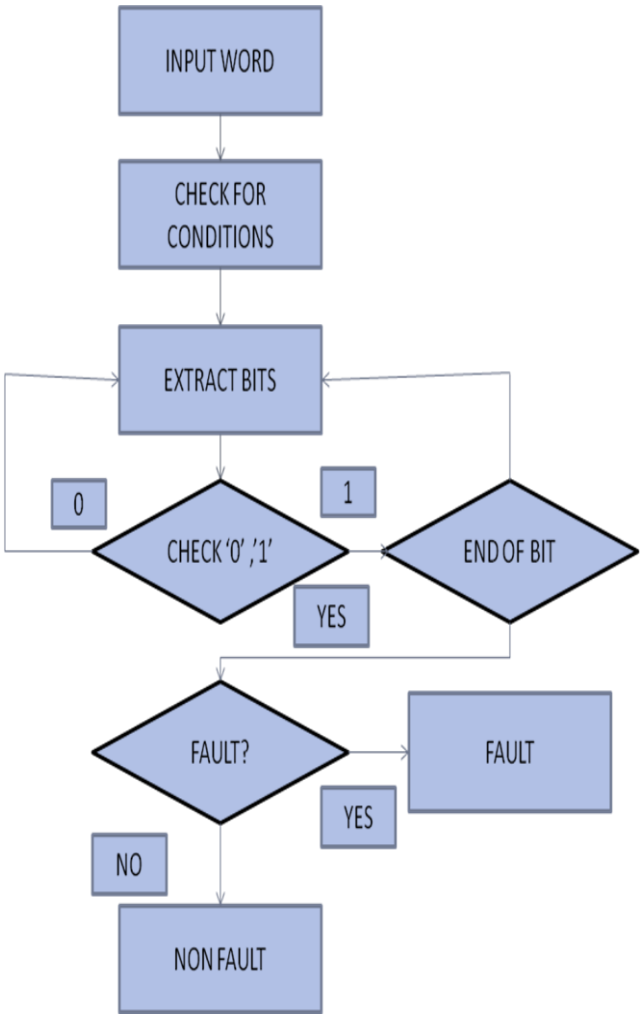


Fig 1. Block diagram



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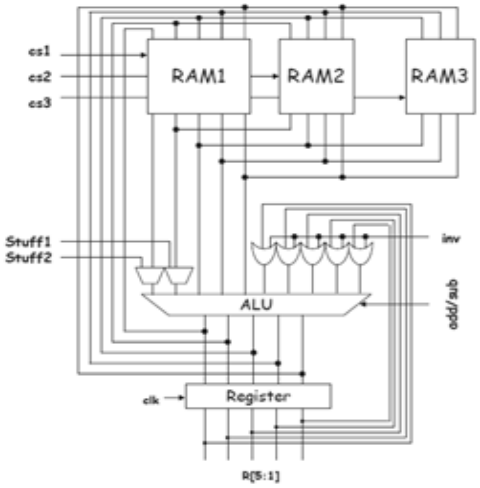

Fig 3. Transparent testing of RAM modules with different word width.

Fig 2 Flow diagram

3.1 Transparent online BIST for an array of RAM modules:

For the case of three RAM modules, having different word width with 3, 4 and 5 bits each, are to be tested transparently online in a roaming manner using a 5 stageALU. The RAM to be tested is enabled through the cs1,cs2 or cs3 chip select signal. When the RAM1 is tested, the inputs of the ALU are driven by the outputs of the RAM1; when RAM2 is tested, the higher order input of the ALU is driven by the stuff2 signal; when RAM3 is tested, the two high order inputs are driven by the signals stuff1 and stuff2.

IV EXPERIMENTAL RESULTS

The design is being simulated using Xilinx 14.2. The simulation results are shown below.

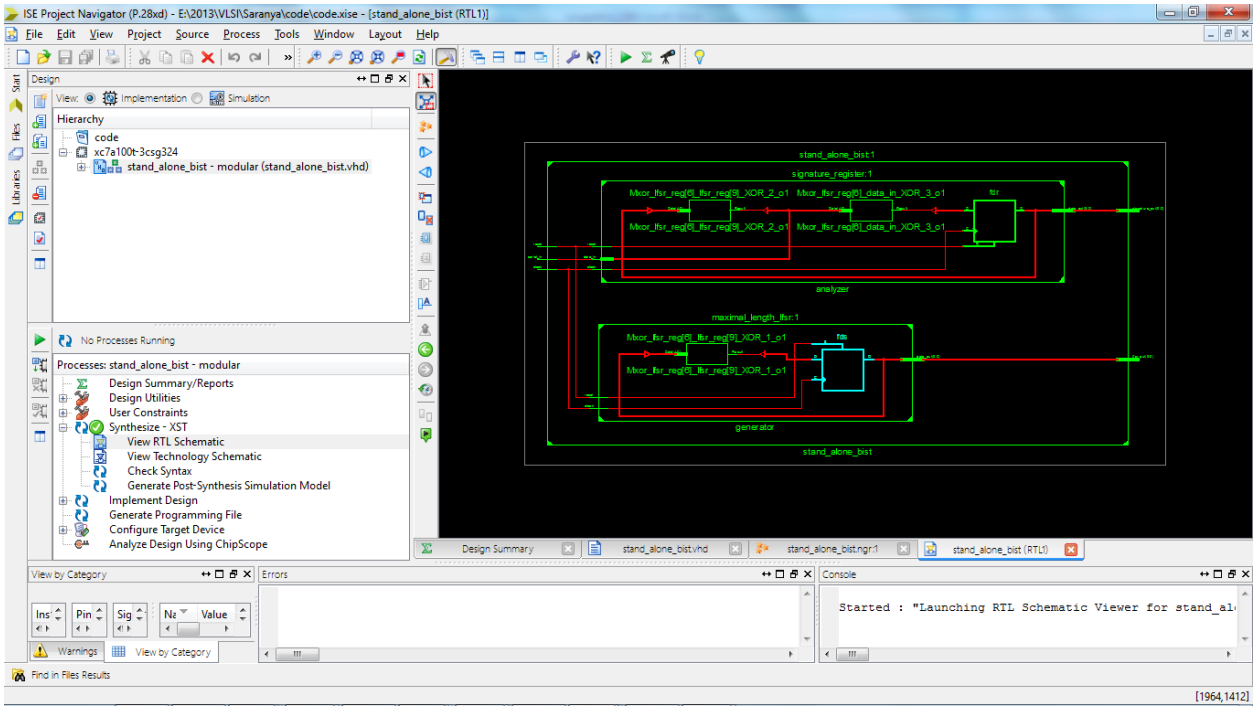

Fig 4. Schematic diagram

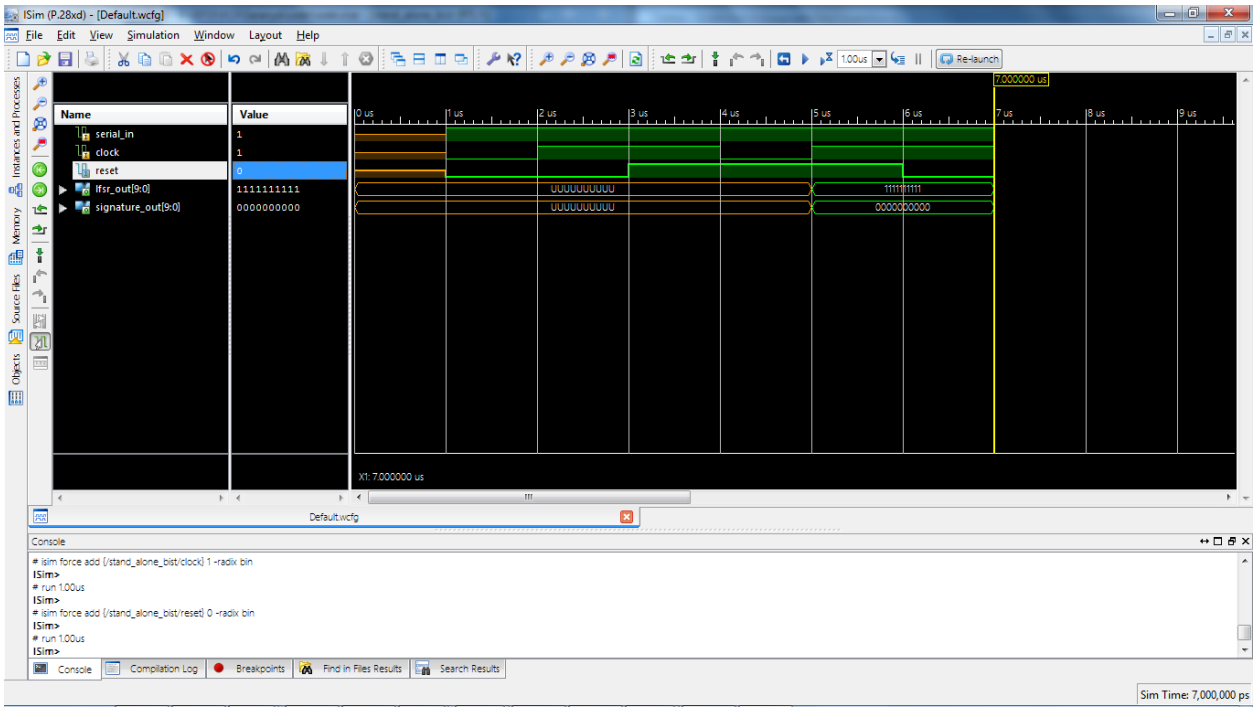

Fig 5. BIST simulation vector waveform

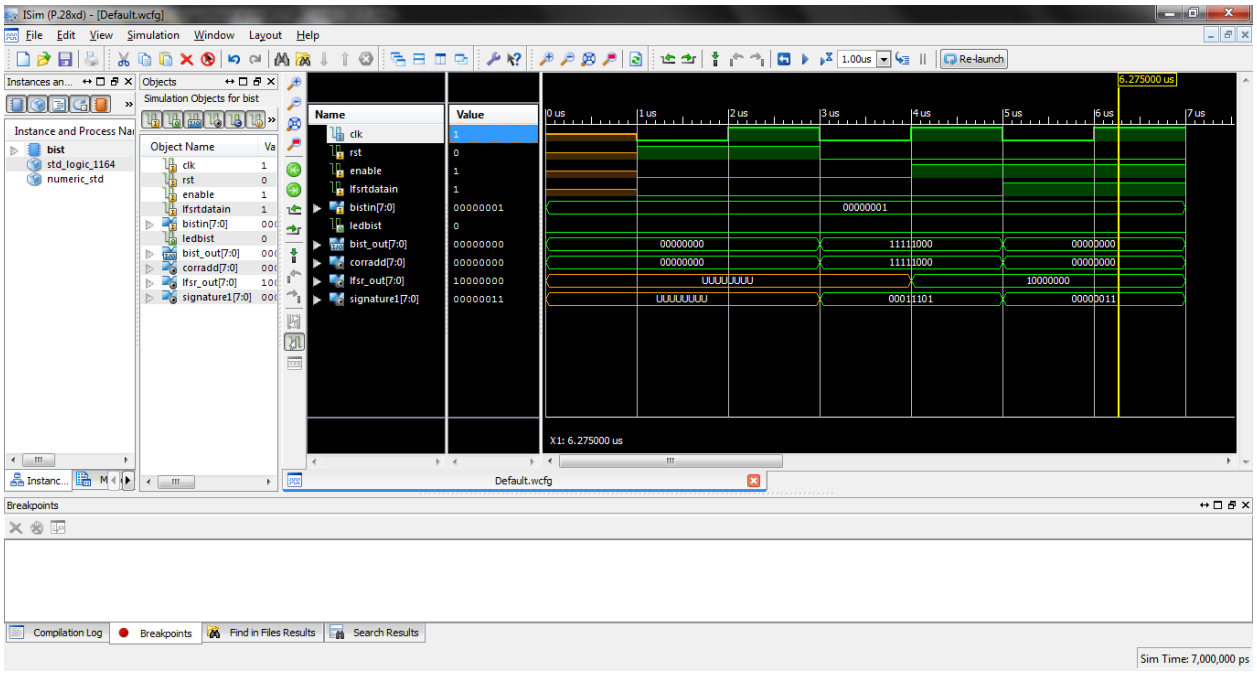

Fig 6. RAM simulation Vector waveform

V CONCLUSION

In this paper testing of RAM modules has been presented using the symmetric transparent principle. This scheme tests a RAM utilizing an ALU module whose number of stages can be larger than the word width and that can be used to test an array of RAM modules where the largest RAM word width does not exceed the number of stages of ALU.

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